Specification

EPD-Module
Part-No. 89008801

1.5", 188 ppi, single sided driven, B/W

Revision 1.01

E-PI Confidential

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1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the electrophoretic display module, part number 89008801. It defines general characteristics of the display module and the technical information required to integrate the display module into a potential product.

The 89008801 is an active-matrix electrophoretic display (AM EPD), with interface and a reference system design. The 1.5" active area contains 200 x 200 pixels and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU-interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. The module can be used in portable electronic devices, such as electronic shelf label (ESL) systems.

1.2 Key features of display module

- Consists of an active-matrix electrophoretic display driven by one chip combining source drivers, gate drivers, controller and display-RAM bonded directly on the display substrate (COG = chip on glass)
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, gate and source driving voltages
- I^2C signal master interface to read an external temperature sensor
- Serial peripheral interface available
- 200 x 200 pixels @ 135 µm pixel pitch
- Supports black and white
- Incorporates industry-leading bi-stable electrophoretic display technology in pure reflective mode and with ultra-wide viewing angle
- Ultra-low power consumption and ultra-low current sleep mode
- White reflectance above 45 %
- Contrast ratio above 20 : 1

2. Mechanical specification

2.1 Dimensions

Parameter	Value	Unit	Comments
Active area size	1.5	inch	
Active area dimension	27.00 x 27.00	mm	
Active area resolution	200 x 200 188	Pixel ppi	
Active area pixel pitch	135	µm	
Outline length	37.32 ± 0.2	mm	
Outline width	31.80 ± 0.2	mm	
Thickness	0.82 ± 0.1	mm	
FPC-length	14.30 ± 0.3	mm	length over display outline
Weight	2.1	g	typical

Table 1: Mechanical specification

2.2 Outline

The outline of the final product is depicted in Figure 1.

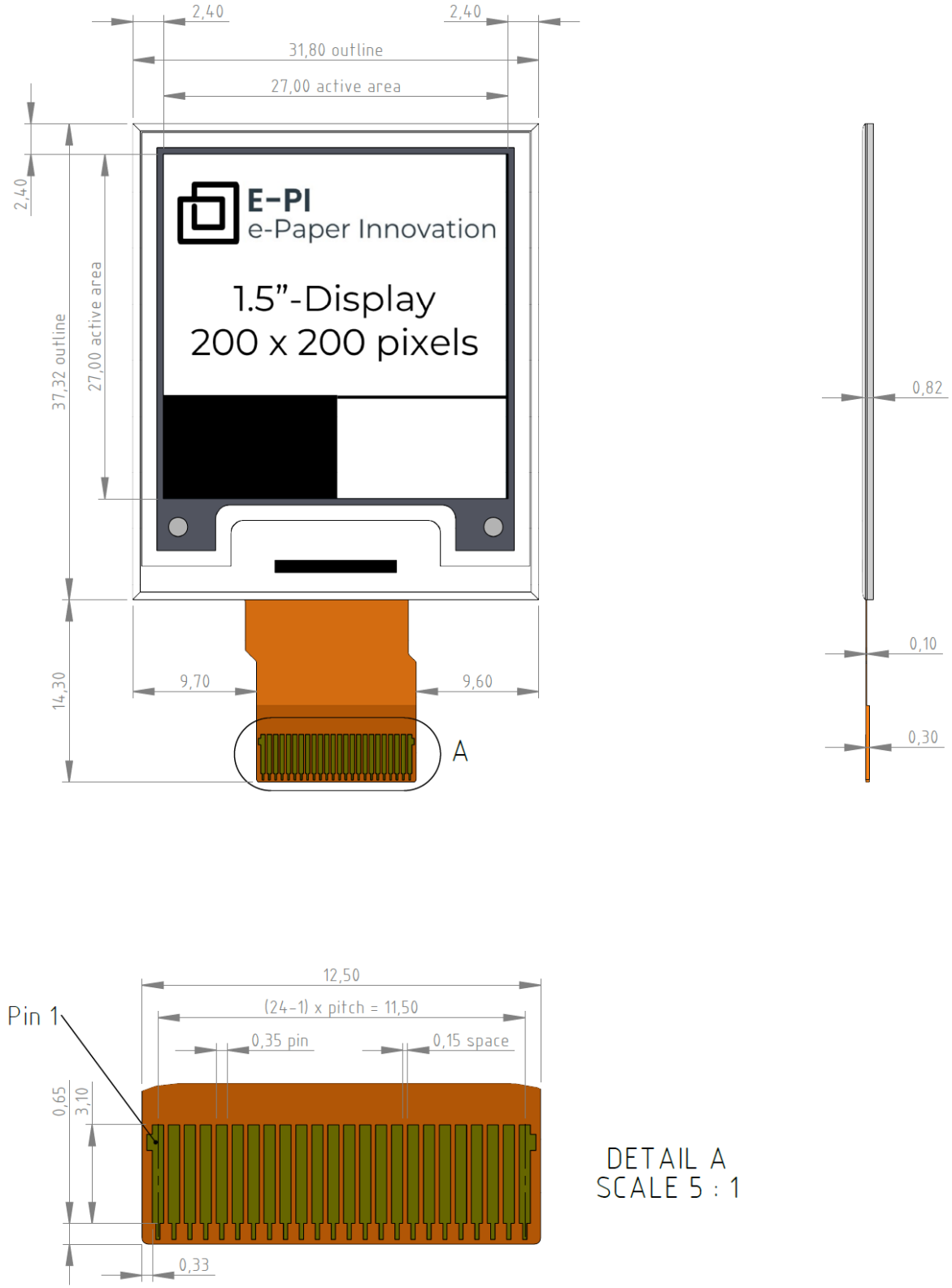


Figure 1: Dimensions of the final product in mm

3. Optical specification

The display supports natively black and white. Specific display grey levels are defined using the terminology GLx, where x = 0-15. GL0 corresponds to “black” and GL15 corresponds to “white”.

Grey levels are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and Lw are measured in % reflectance and Lw is defined as 100 %. This formula is valid for L* > 16.

Measurements are made with illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

3.1 Optical requirements

3.1.1 Picture quality

The display will be lineout free; however typical expectations are a pixel yield of > 99.99 %.

3.1.2 Parameters for GL waveforms

Parameter	Description	Min	Typical	Max	Unit
White state	Median GL15	73	75	-	L*
Black state	Median GL0	-	16	18	L*

Table 2: Optical requirements

3.1.3 Display update waveforms

The display module will be supplied with a library of waveforms that are tuned to optimise display performance. The waveform library will be stored into an on-board flash memory. Each waveform has an optimum temperature range over which it is valid – it is the responsibility of the display controller in combination with an on-board temperature sensor to ensure that the correct waveform is selected for the current display module temperature.E-PI will provide the waveforms that support full screen updates as well as partial updates, see Table 3.

Waveform type	Typical update time at 23°C[1]	Comments
Standard full refresh[2]	750 ms	Drives all pixels from its original value to its target value (via the black and/or white state); the screen will flicker during the refresh process
Partial refresh	250ms	The screen does not flicker during the refresh process

Table 3: Waveform types

[1] Does not include time required to initialise power supplies or drive initial null frame to display.

[2] Initialisation of the display should be achieved by applying two standard updates to a white target image. This would typically be used when recovering from a serious system error where the state of the display is unknown.

4. Reliability and other specifications

Parameter	Value	Unit	Comments
Operating Temperature Range	0 to 50	°C	The operating temperature of 0 to 50 °C is a limitation of the media material
Operating Humidity Range	Max 70	%RH	
Operation Illuminance Intensity	Max 2000	Lux	Indoor use
Storage Temperature Range	-25 to 60	°C	30%RH to 60%RH
Waterproofing	n/a		The deliverables of this product will not guarantee an IP rating

Table 4: Reliability parameters

No.	Test	Condition	Method
1	High Temperature Operation	T = +50°C, RH = 30 % for 168 hrs	IEC 60 068-2-2Bp
2	Low Temperature Operation	T = 0°C for 168 hrs	IEC 60 068-2-2Ab
3	High Temperature Storage	T = +70°C, RH = 23 % for 168 hrs	IEC 60 068-2-2Bp
4	Low Temperature Storage	T = -25°C for 168 hrs	IEC 60 068-2-1Ab
5	High Temperature, High Humidity Operation	T = +40°C, RH = 90 % for 168 hrs	IEC 60 068-2-3CA
6	High Temperature, High Humidity Storage	T = +60°C, RH = 80 % for 168hrs	IEC 60 068-2-3CA
7	Thermal Shock	Cycle: [-25°C/30min] → [+70°C/30 min] 100 cycles	IEC 60 068-2-14
8	Package Vibration	1.04 G, frequency: 10 ~ 500 Hz Duration 1 hour in direction X, Y and Z, each	Full packed for shipment
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment
10	Electrostatic Effect (nonoperating)	Machine model +/- 250 V, 0 Ω, 200 pF	IEC 62179, IEC 62180

Table 5: Reliability tests; at the end of the test, electrical, mechanical, and optical specifications shall be fulfilled

5. Electrical Specification

5.1 Connection of display module

The display module can be contacted by a FPC bonded to the backplane. The contacts are on the frontside of the FPC. Dimensions are shown in Figure 1. On the connector side, The FPC has a 5.85 mm deep stiffener resulting in a 0.3 mm thick FPC on the connector side. There are 24 Pins having a pitch of 0.5 mm.

5.2 Electrical pin-out of display module

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

Table 6: Electrical pin-out to connect the display module

I = Input Pin O =Output Pin I/O = Bi-directional Pin (Input/Output)

P = Power Pin C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., the chip would put Busy pin High when

- Outputting display waveform,
- Programming with OTP or
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin:

BS-state Low: 4-lines serial peripheral interface (SPI)

BS-state High: 3-lines serial peripheral interface (SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{dd} +0.5	V
Logic Output voltage	VOUT	-0.5 to V_{dd} +0.5	V

Table 7: Maximum ratings

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the panel DC characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS = 0V, VDD = 3.0V, T_{OPR} = 25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{dd}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100 µA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100 µA	-	-	-	0.1 V_{dd}	V
OTP Program voltage	V_{PP}	-	VPP	-	7.5	-	V
Typical power panel	PTYP	-	-	-	12	30	mW
Deep sleep mode	PSTPY	-	-	-	3	-	µW
Typical operating current	Iopr_VDD	V_{dd} = 3.0 V-	-	-	4.0	10	mA
Sleep mode current	Islp_VDD	VDD = 3.0 V DC/DC OFF No clock No output load RAM data retain	VDD	-	20	--	µA

Deep sleep mode current	IdslpVDD	VDD = 3.0 V DC/DC OFF No clock No output load RAM data not retained	VDD	-	1	--	µA

Table 8: Panel DC characteristics

Notes:

1. The typical power is measured with following transition: from horizontal 2 grey scale pattern to vertical 2 grey scale pattern, see Figure 2.
2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E-PI

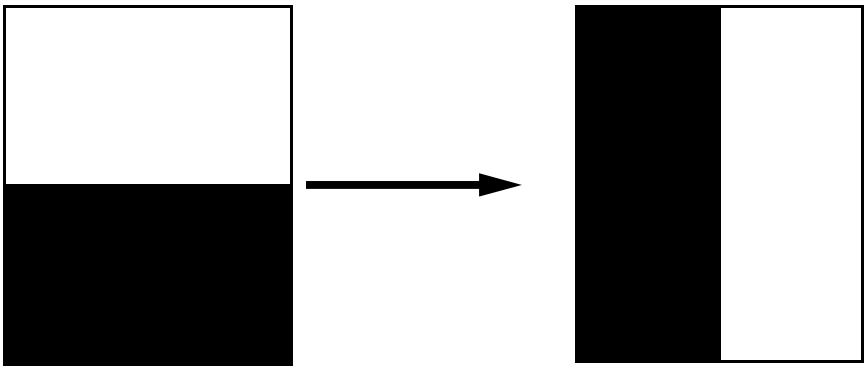


Figure 2: pattern for power consumption measurement

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 9. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	D/C	RSTN
4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI	SDIN	SCLK	CSB	L	RSTN

Table 9: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Table 10: Control pins of 4-wire serial interface

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, … D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

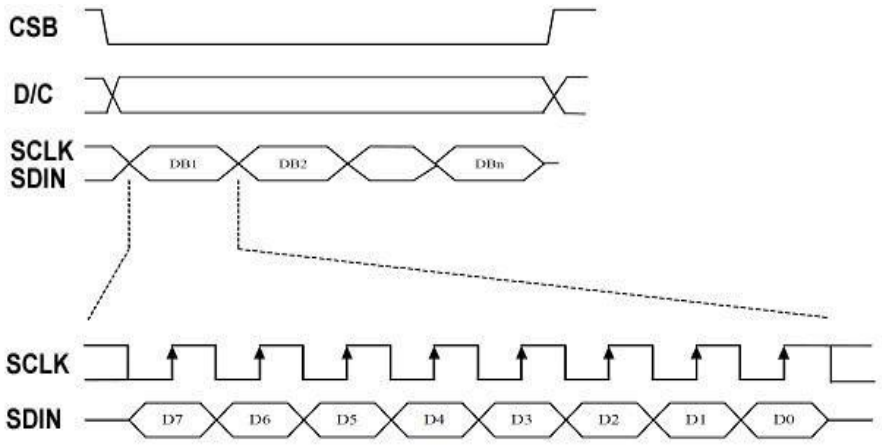


Figure 3: Write procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0)

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	LOWTie	↑

Table 11: Control pins of 3-wire serial interface

Note：↑ stands for rising edge of signal [LOW]

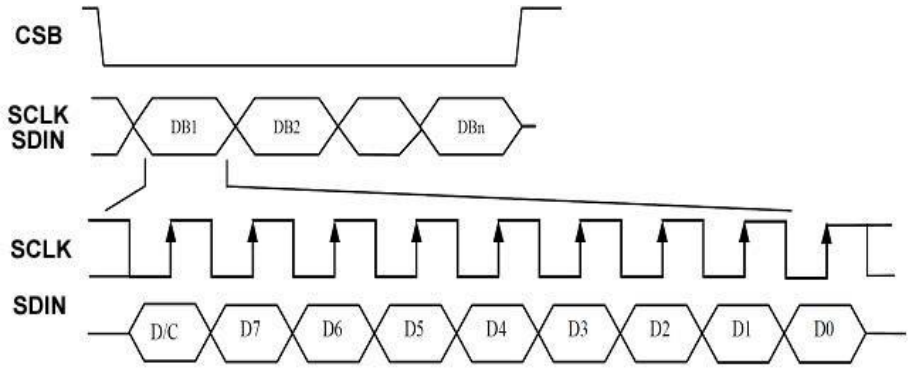


Figure 4: Write procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for VSS = 0.0 V, VDD = 3.0 V, T_{OPR} = 25°C.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal oscillator frequency	VDD = 2.4 to 3.3V	CL	0.95	1.00	1.05	MHz

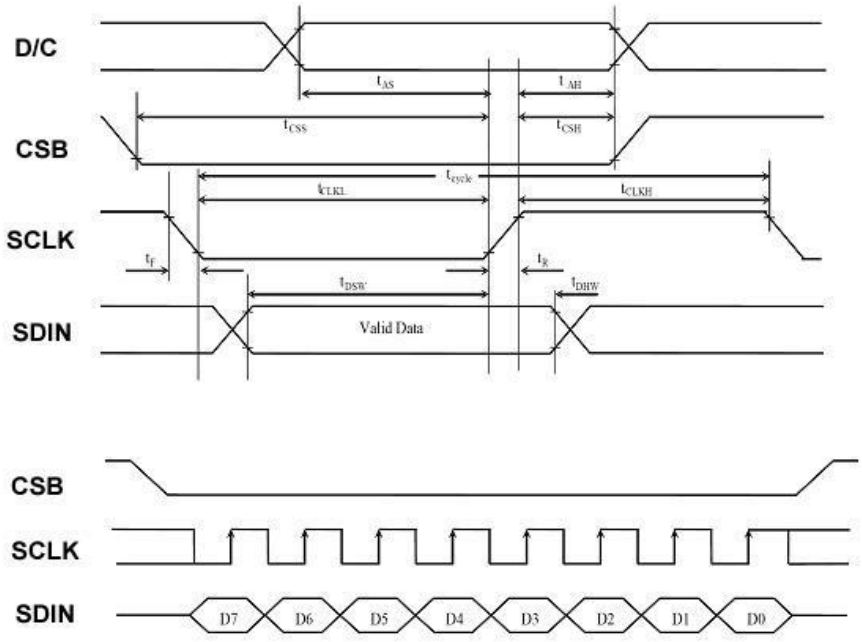


Figure 5: Serial interface characteristics

(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tcycle	Clock Cycle Time	250	-	-	ns
tAS	Address Setup Time	150	-	-	ns
tAH	Address Hold Time	150	-	-	ns
tCSS	Chip Select Setup Time	120	-	-	ns
tCSH	Chip Select Hold Time	60	-	-	ns
tDSW	Write Data Setup Time	50	-	-	ns
tDHW	Write Data Hold Time	15	-	-	ns
tCLKL	Clock Low Time	100	-	-	ns
tCLKH	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

Table 12: Serial interface timing characteristics

7. Block Diagram

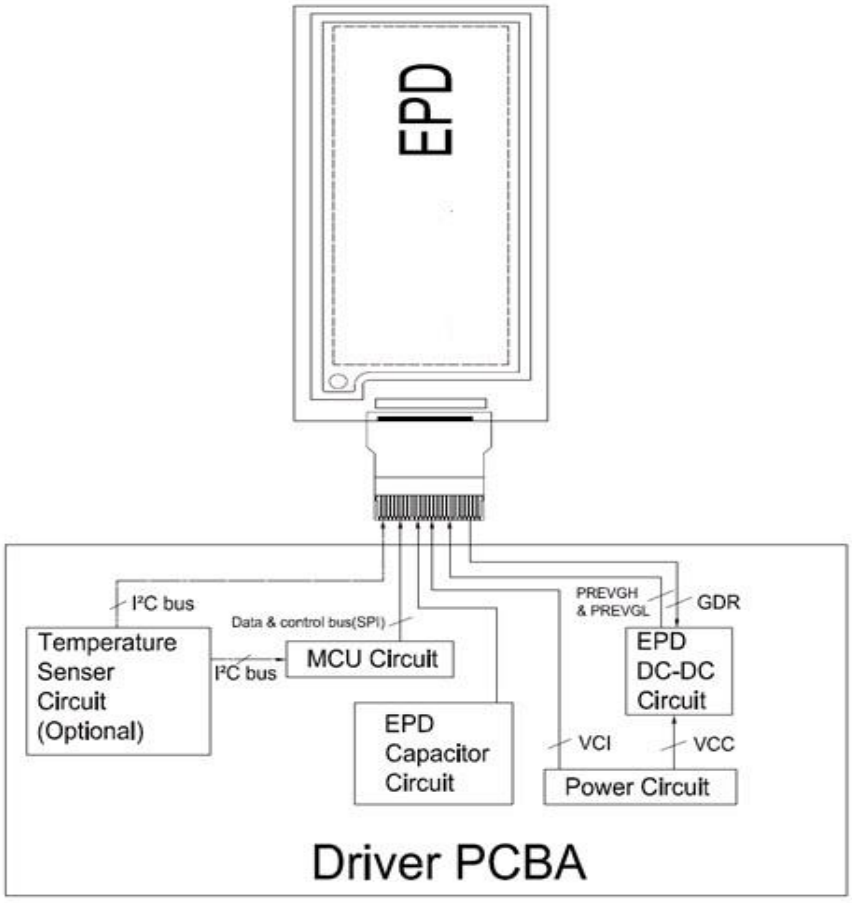


Figure 6: Block diagram

8. Application reference circuit for display module

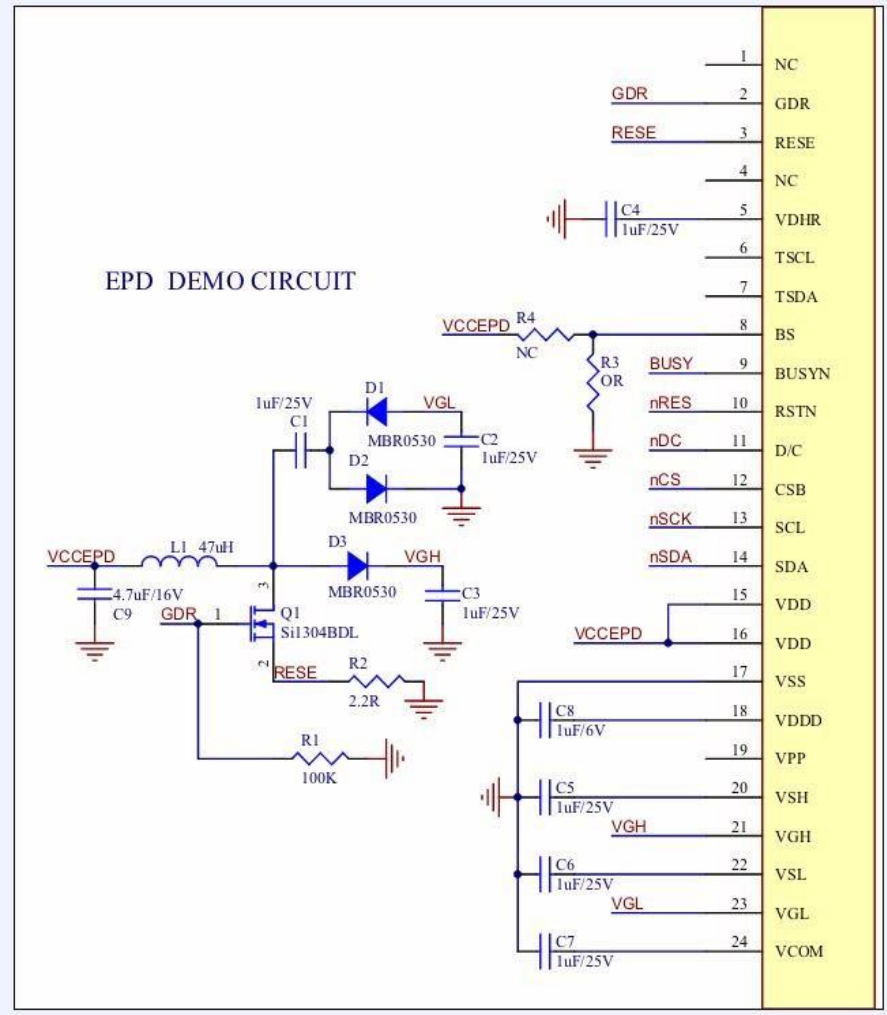


Figure 7: Reference circuit

Components	Value/Type	Requirements
C1-C8	1 μF	Dielectric：X5R/X7R, Rated Voltage：25 V
C9	4.7 μF	Dielectric：X5R/X7R, Rated Voltage：25 V
D1-D3	Diode	MBR0530 (1. reverse DC ≥ 30 V / 2. Io ≥ 500 mA / 3 .forward ≤ 430 mV)
R1	100 kΩ	1 %
R2	2.2 Ω	1 %
Q1	NMOS	Si1304BDL 1.Drain Source breakdown voltage ≥ 30 V 2.Vgs(Vth) = 0.9 V（TYP）,1.3 V(Max) 3. Rds on ≤ 2.1 Ω @Vgs = 2.5 V
L1	47 μH	CDRH2D18/LDNP-470NC, Io = 500(Max)

Table 13: Reference components

9. Handling requirements

The display modules are shipped in appropriate packages. All loose tails must be constrained during shipping.

Keep the EPD-panel/module in the specified environment and original packing boxes when stored to avoid scratching and to keep original performance.

The product is intended to be used around ambient temperature. Please control the temperature to avoid frost or dew on the surface of EPD-panel. Moisture may ingress the EPD-panel and may damage the EPD-panel.

High temperature, high humidity, sunlight, or UV-light may degrade the EPD-panel's performance. Please do not expose the unprotected EPD-panel to high temperature, high humidity, sunlight, or UV-light for long periods of time. Please store the EPD panel in controllable environment of warehouse and in original package, without sunlight, without condensation.

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode the electronic components.

Do not disassemble or re-assemble the EPD-panel.

The EPD panel/module is manufactured from fragile materials such as glass and plastic and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating.

Minimise pulling or bending of the FPC and do not use the FPC for pick up. Do not press or pull FPC to ± 90° bending and don't twist FPC and PCB. Keep r ≥ 1mm when bending for assembly.

To avoid scratches, do not stack the EPD-panels/modules.

Do not apply pressure or hit to the EPD-module, IC, FPC and PCB to prevent damage.

Do not touch the FPC lead contacts and IC area to avoid ESD damage.

The display module is an electrostatic discharge (ESD) sensitive device. Ensure that proper ESD-precautions are in place to avoid damage of the display module.

Typical operation conditions in the assembly area are (25 ± 2)°C and 50%RH to 60%RH. Operators should use ionizer fan during assembly. The working area must be connected to ground, the resistance between operator and working area should be less than 5 Ω. Operator should wear PVC or anti-electrostatic gloves. Operators should wear grounding wrist ring and must make sure that grounding is fine. Before working in operation area, please ensure wrist ring and suit is fine by passing a conductive test before operation.

To avoid electrical overstress (EOS) in operation, please

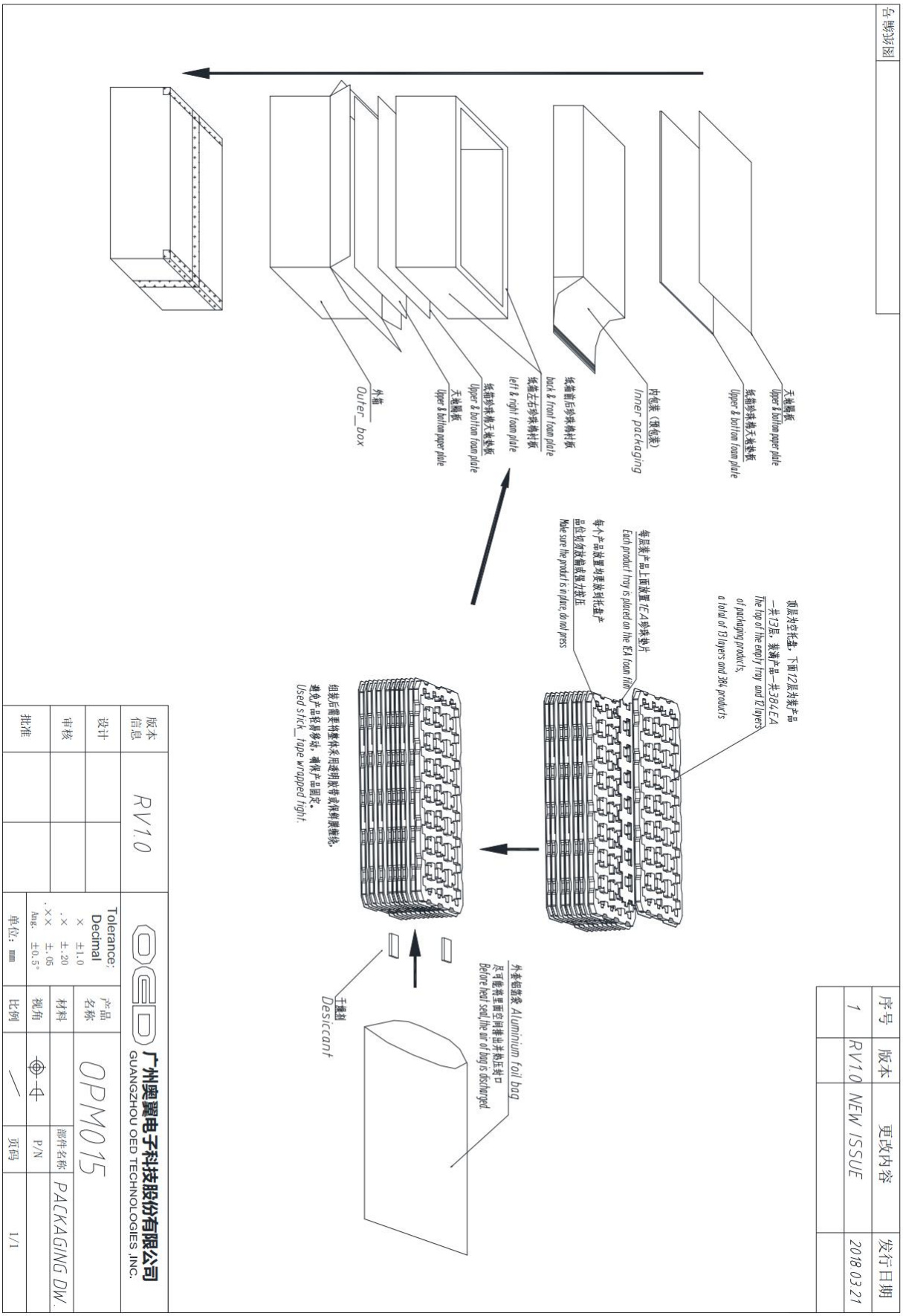
- ensure that power is off before EPD is installed into jig/tag
- ensure that FPC is well connected (no misalign in connector) to avoid a short
- do not remove/uninstall EPD from jig/tag when image is updating,
- switch power off after operation or function test before uninstalling the EPD

EOS or short may damage the IC or the TFT.

10. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

11. Packaging



12. Mark and Bar Code Definition

OPM015C6 YYYMMDD XX

YZC030AN1001001

A. OPM015C6: Module No.
B. YYYYMMDD: Product date year month day
C. XX: Internal Code
D. Bar Code definition

YZC030 A N1 001 001

（1） （2） （3） （4） （5）

1. O-Paper Film lot
2. Factory
3. Internal Code
4. Product lot
5. Product serial number

13. Inspection Standard

13.1 Appearances Inspection Standard

This appearance inspection shall be applied to EPD modules.

13.1.1 Inspection Conditions

Viewing Angle:	α = ± 45°
Viewing Distance:	30 cm ± 10 cm
Ambient Luminance:	700 ~ 1000 Lux
Supply Voltage:	typical value described on the electrical characteristics
Environment:	ambient temperature 20℃ ~ 25℃
ambient humidity	40 ~ 70%RH

ESD should be controlled within ± 200 V

13.1.2 Inspection Level: Level II

Sampling table: GB/T 2828.1-2012 II, unless otherwise agreed in writing.

13.1.3 Acceptance Quality Level (AQL)

major defect: 0.65

minor defect: 1.5

13.1.4 Classification of Defects

Defects are classified as either a major or a minor defect defined as below.

A major defect is a defect that is likely to result in failure or to significantly reduce the usability of the product for the intended function.

A minor defect is a defect that will not result in functional problems or classified deviations.

13.2 Quality Criteria

13.2.1 Zone Definitions

A-zone: EPD active area (not including border)
B-zone: out of active area

13.2.2 Appearances Criteria

The criteria are shown in the tables below. If any other items, values or applicable zones need to be required to be defined, a written agreement shall be signed, and otherwise a limited sample shall be made for reference.

Item	Description	Classification
No Image	No image shown on screen due to malfunction	Major
Line Missing	Line missing	Major
Abnormal Display	Unusual pattern or function displayed	Major
TFT Broken	TFT broken by external force	Major

Table 14: Major defects

Item		Criteria	Specific Zone	
Name	Description		A Zone	B Zone
Dot defect	spot, air bubble, foreign material in dot shape	D ⩽ 0.30 mm	Ignore	Ignore
		0.30 mm ＜ D ⩽ 0.50 mm	⩽5	
		D ＞ 0.50 mm	0	
Line defect	scratch on top surface, foreign material in line or spiral shape	L ⩽ 1.0 mm & W ⩽ 0.15mm	Ignore	Ignore
		1.0 mm ＜ L ⩽ 5.0 mm & 0.15mm ＜ W ⩽ 0.5 mm	⩽4	
		L ＞ 5.0 mm or W ＞ 0.5mm	0	
Chipping	corner chip	Do not affect the display, do not have diffuse or comminute cracks		
	edge chip			
Curl	curl for panel	⩽ 1.0 mm		

Table 15: Minor defects

A dot is defined as L ≤ 0.5 mm and L <4 W. Otherwise, it is a line defect, see Figure 8. A chip is a small area with missing material at the edges of the display module, see Figure 9.

Figure 8: line defect (left) and dot (right)

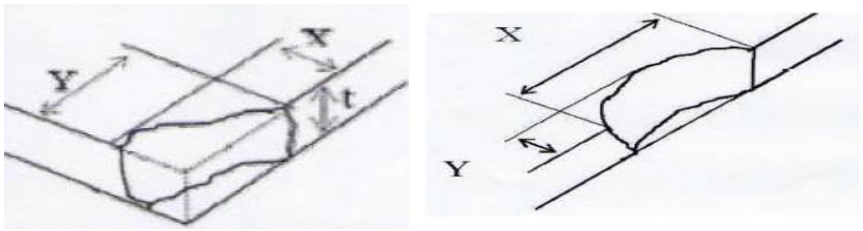


Figure 9: Corner chip (left) and edge chip (right)