Specification

EPD-Module
Part-No. 89005802

10.3", 135 ppi, single sided driven, Colour

Revision 1.00

E-PI Confidential

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1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the electrophoretic display module, part number 89005802. It defines general characteristics of the display module and the technical information required to integrate the display module into a potential product.

The 89005802 is an active-matrix electrophoretic display (AM EPD), with interface and a reference system design. The 10.3" active area contains 2240 x 1680 pixels driving a 16GL-EPD. On top of the media, a colour filter array is positioned so that 4096 colours can be displayed with a resolution of 1120 x 840 pixels. The module can be used in portable electronic devices e.g. E-book readers.

1.2 Key features of display module

- Consists of an active-matrix electrophoretic display with integrated circuit including source drivers and gate drivers
- 1120 x 840 pixels @ 187 µm pixel pitch
- Supports 4096 colours
- Incorporates industry-leading bi-stable electrophoretic display technology in pure reflective mode and with ultra-wide viewing angle
- Ultra-low power consumption
- White reflectivity typically 20 %
- contrast ratio typically 18 : 1
- Supports landscape and portrait modes

2. Mechanical specification

2.1 Dimensions

Parameter	Value	Unit	Comments
Active area size	10.3	inch	4 : 3 aspect ratio
Active area dimension	209.66 x 157.25	mm	
Active area resolution	1120 x 840 135	Pixel ppi	
Active area pixel pitch	187	µm	
Outline length	216.70 ± 0.2	mm	
Outline width	174.40 ± 0.2	mm	
Thickness	0.72 ± 0.1	mm	
FPC-length	45.32 ± 0.3	mm	length over display outline
Weight	70	g	typical

Table 1: Mechanical specification

2.2 Outline

The outline of the final product is depicted in Figure 1.

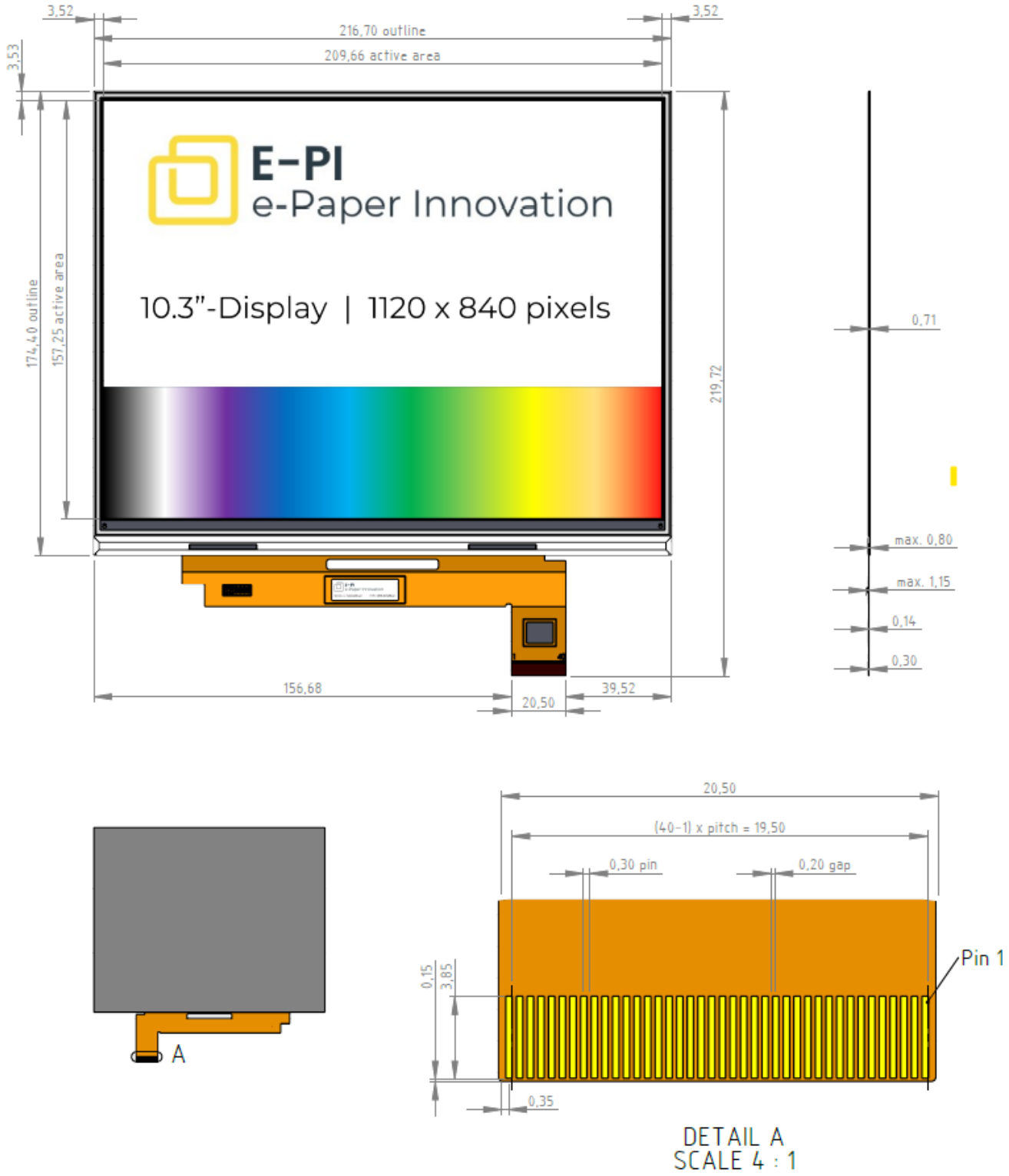

Figure 1: Dimensions of the final product in mm

3. Optical specification

The display supports natively black and white. Specific display grey levels are defined using the terminology GLx, where x = 0-15. GL0 corresponds to “black” and GL15 corresponds to “white”.

Grey levels are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and Lw are measured in % reflectance and Lw is defined as 100 %. This formula is valid for L* > 16.

Measurements are made with illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

3.1 Optical requirements

3.1.1 Picture quality

The display will be lineout free; however typical expectations are a pixel yield of > 99.99 %.

3.1.2 Parameters for GL waveforms

Parameter	Description	Min	Typical	Max	Unit
White state	Median GL15		52	-	L*
Black state	Median GL0	-	10	-	L*
Colour gamut	Acc. NTSC		≥ 5		%

Table 2: Optical requirements

3.1.3 Display update waveforms

The display module will be supplied with a library of waveforms that are tuned to optimise display performance. The waveform library can be stored into a flash memory. Each waveform has an optimum temperature range over which it is valid – it is the responsibility of the display controller in combination with an on-board temperature sensor to ensure that the correct waveform is selected for the current display module temperature. E-PI will provide the waveforms, see Table 3.

Waveform type	Typical update time at 23°C[1]	Comments
Standard full refresh[2]	520 ms	Drives all pixels from its original value to its target value (via the black and/or white state); the screen will flicker during the refresh process
Partial refresh	250ms	On request

Table 3: Waveform types

[1] Does not include time required to initialise power supplies or drive initial null frame to display.

[2] Initialisation of the display should be achieved by applying two standard updates to a white target image. This would typically be used when recovering from a serious system error where the state of the display is unknown.

4. Reliability and other specifications

Parameter	Value	Unit	Comments
Operating Temperature Range	0 to 50	°C	The operating temperature of 0 to 50 °C is a limitation of the media material
Storage Temperature Range	-20 to 70	°C	30%RH to 60%RH
Waterproofing	n/a		The deliverables of this product will not guarantee an IP rating

Table 4: Reliability parameters

No.	Test	Condition	Method
1	High Temperature Operation	T = +50°C, RH = 30 % for 240 hrs	IEC 60 068-2-2Bp
2	Low Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab
3	High Temperature Storage	T = +70°C, RH = 23 % for 168 hrs	IEC 60 068-2-2Bp
4	Low Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab
5	High Temperature, High Humidity Operation	T = +40°C, RH = 90 % for 168 hrs	IEC 60 068-2-3CA
6	High Temperature, High Humidity Storage	T = +60°C, RH = 80 % for 240hrs	IEC 60 068-2-3CA
7	Thermal Shock	Cycle: [-25°C/30min] → [+70°C/30 min] 100 cycles	IEC 60 068-2-14
8	Package Vibration	1.04 G, frequency: 10 ~ 500 Hz Duration 1 hour in direction X, Y and Z, each	Full packed for shipment
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment
10	Electrostatic Effect (nonoperating)	Machine model +/- 250 V, 0 Ω, 200 pF	IEC 62179, IEC 62180

Table 5: Reliability tests; at the end of the test, electrical, mechanical, and optical specifications shall be fulfilled

5. Electrical Specification

5.1 Connection of display module

The display module can be contacted by a FPC bonded to the backplane. The contacts are on the backside of the FPC. Dimensions are shown in Figure 1. On the connector side, The FPC has a

5.0 mm deep stiffener resulting in a 0.3 mm thick FPC on the connector side. There are 40 Pins having a pitch of 0.5 mm.

5.2 Electrical pin-out of display module

No.	Name	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	NC	NO Connection
5	VDD	Digital power supply drivers
6	GMODE1	Output mode selection gate driver
7	CPV	Shift clock input
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM	Common connection
11	VDD	Digital power supply drivers
12	VSS	Ground
13	CLK	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	SPH	Start pulse source driver
32	LE	Latch enable source driver
33	OE	Output enable source driver
34	NC	NO Connection
35	NC	NO Connection

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36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	NC	NO Connection
40	VBORDER	Border connection

Table 6: Electrical pin-out of the connectors

6. Electrical Characteristics

6.1 Module Interface Description

This module can be driven by HH7163 timing controller (T-Con).

6.2 Module DC Characteristics

The following specifications apply for: VSS = 0V, VDD = 3.0V, T_{OPR} = 25°C.

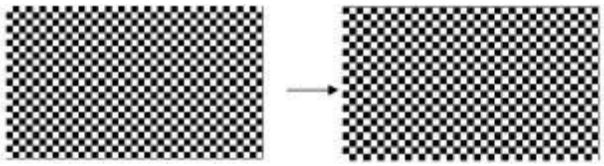
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal ground	VSS		-	0	-	V
Logic Voltage supply	VDD		3.0	3.3	3.6	V
	IVDD	VDD = 3.3 V	-	4.0	6.5	mA
Gate Positive supply (*A)	VGH		27	28	29	V
	IVGH	VGH = 28 V	-	1.1	1.2	mA
Gate Negative supply	VGL		-21	-20	-19	V
	IVGL	VGL = -20 V	-	1.0	13.5	mA
Source Positive supply	VPOS		14.6	15	15.4	V
	IPOS	VPOS = 15 V	-	1.0	81	mA
Source Negative supply	VNEG		-15.4	-15	-14.6	V
	INEG	VNEG=-15V	-	1.0	81	mA
Asymmetry source	VASYM	VPOS+VNEG	-800	0	800	mV
Common voltage	VCOM		-2.0	-1.0	-0.8	V
	ICOM		-	0.2	0.2	mA
Standby power module	PSTBY			TBD	TBD	mW
Typical power module	PTYP		-	100	TBD	mW
Operating temperature			0		50	℃
Operating relative humidity	RHop		0		70	%RH
Storage temperature			-20	-	70	℃
Storage relative humidity	RHst		30		60	%RH
Maximum image update time at 25℃			-	450	-	ms

Table 7: Panel DC characteristics

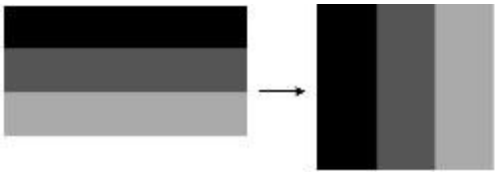
Notes:

1. The maximum power and maximum current are specified for the worst-case power consumption.
2. The typical power is measured when “typical images” are displayed.
3. The standby power is the consumed power when the module controller is in standby mode.
4. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E-PI.
5. (*A) Feedback resistance of main board VGH circuit is updated to 36.3 KΩ ± 0.5 %.

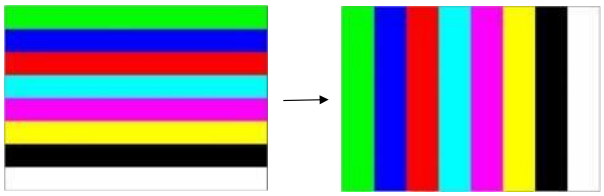
The maximum power consumption



The typical power consumption



The typical power consumption for colour



6.3 Module AC Characteristics

The following specifications apply for VDD = 3.0 V to 3.6 V unless otherwise specified, T_{OPR} = 25°C.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Applicable pin
fcpv	Clock frequency			200	kHz	CPV
tCPVh	Clock CPV high time	0.5	-	-	µs	
tCPVl	Clock CPV low time	0.5	-	-	µs	
tSU	Data setup time	100	-	-	ns	CPV STV
tH	Data hold time	300	-	-	ns	
tclk	Clock CLK cycle time	40	-	-	ns	See below
tsu	D0 .. D7, SPH setup time	8	-	-	ns	
th	D0 .. D7, SPH hold time	8	-	-	ns	
tLEdly	LE on delay time	40	-	-	ns	
tLEw	LE high-level pulse width	40	-	-	ns	
tLEoff	LE off delay time	40	-	-	ns	
tMsu	SHR setup time	100	-	-	ns	
tMh	SHR hold time	10	-	-	ns	

Table 8: Module AC-characteristics

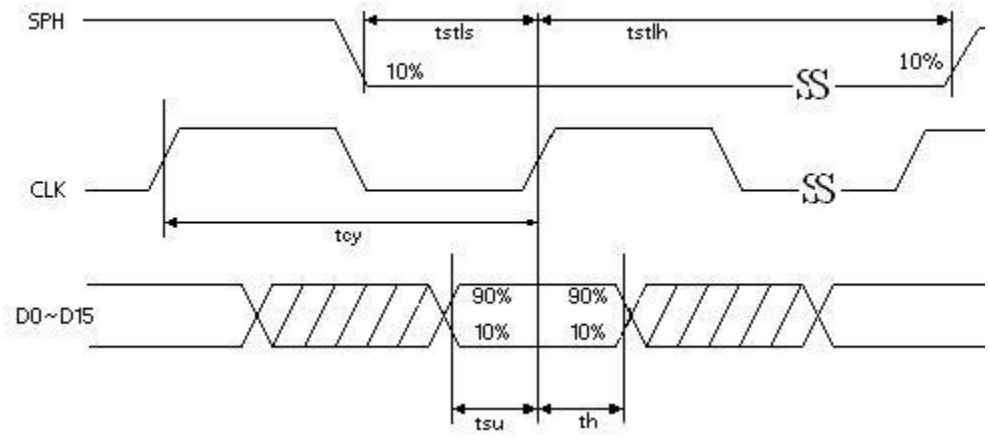


Figure 2: clock and data timings

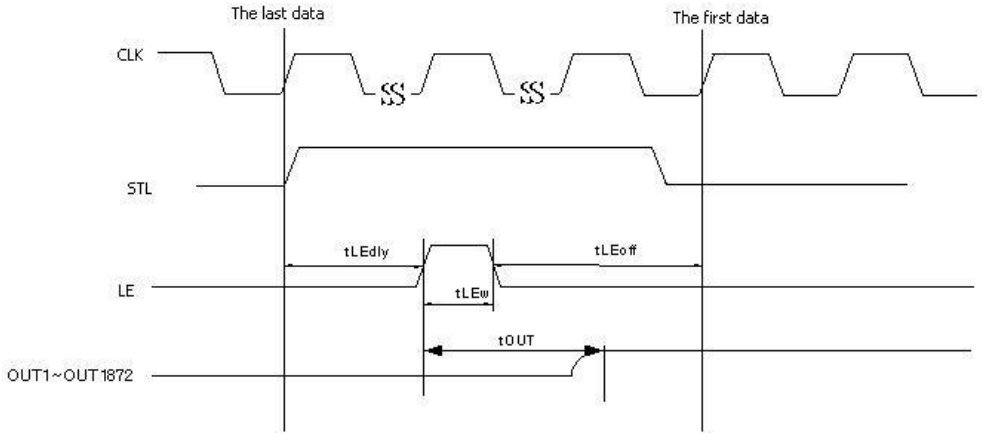


Figure 3: Output latch/control signals

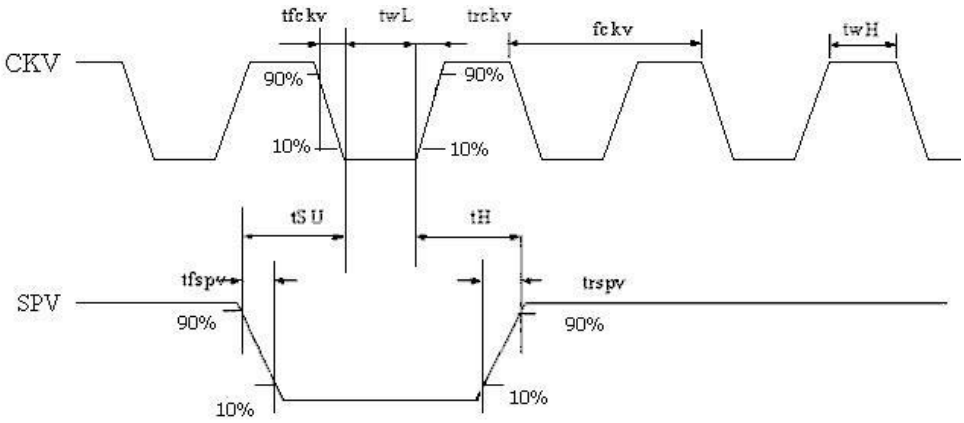


Figure 4: CKV and SPV timing

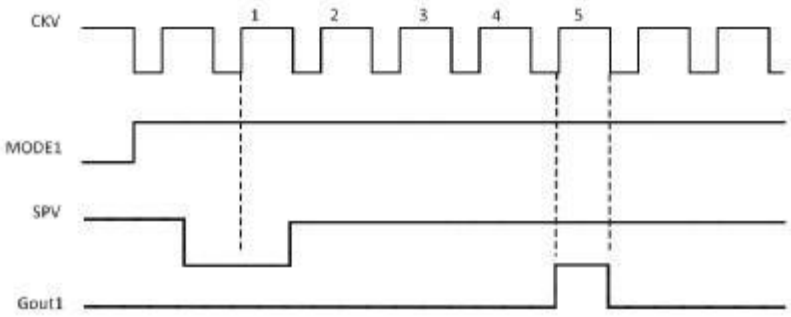


Figure 5: Gate output timing

7. Pixel Arrangement

The colour EPD module pixel arrangement is shown inFigure 6.

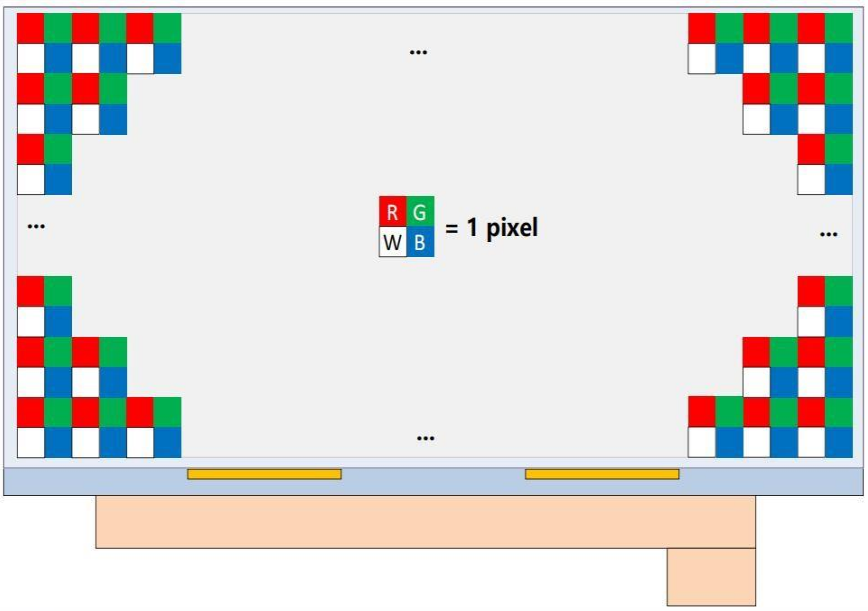


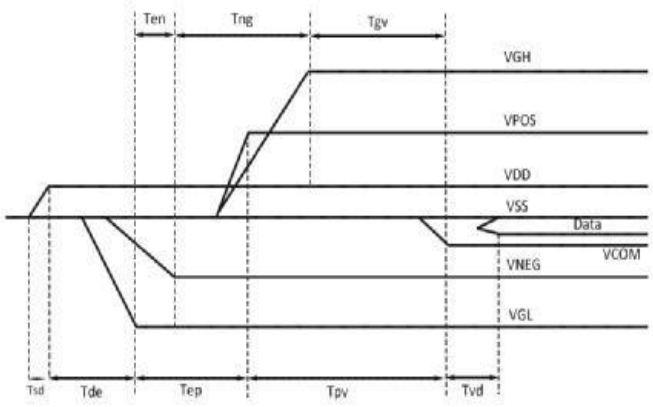
Figure 6: CFA-design

8. Power On/Off Sequence

To prevent the device from damage due to latch up, the power on/off sequence shown below must be followed.

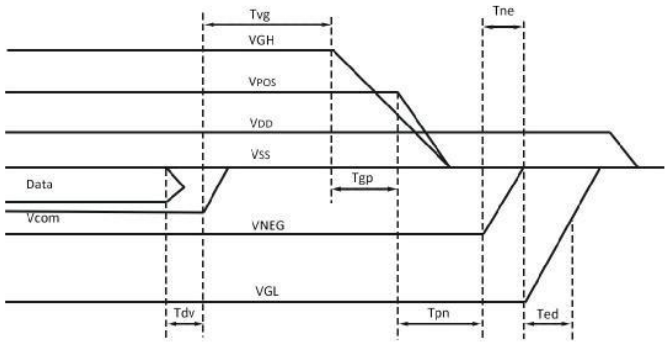
When power on: VDD -> VGL -> VNEG/VGH/VPOS -> Vcom

When power off: Vcom -> VNEG/VGH/VPOS -> VGL -> VDD



Symbol	Min.	Max.	Unit
Tsd	30	-	µs
Tde	100	-	µs
Tep	1000	-	µs
Tpv	100	-	µs
Tvd	100	-	ns
Ten	0	-	µs
Tng	1000	-	µs
Tgv	100	-	µs

Figure 7: Power on sequence



Symbol	Min.	Max.	Unit
Tdv	100	-	µs
Tvg	0	-	µs
Tgp	0	-	µs
Tpn	0	-	µs
Tne	0	-	ns
Ted *	0.5	-	µs

* discharged point @ -7.4 V

Figure 8: Power off sequence

9. Block Diagram

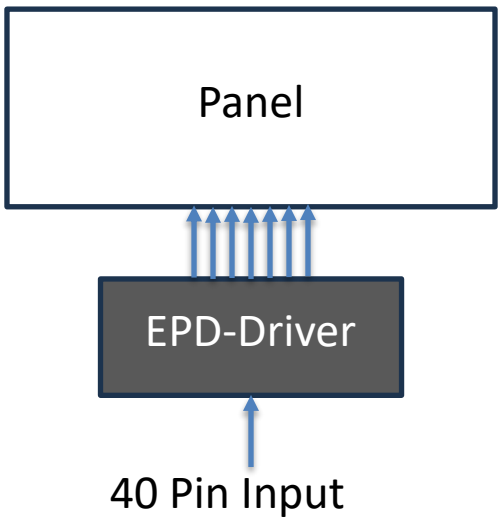


Figure 9: Block diagram

10. Handling requirements

The display modules are shipped in appropriate packages. All loose tails must be constrained during shipping.

Keep the EPD-panel/module in the specified environment and original packing boxes when stored to avoid scratching and to keep original performance.

The product is intended to be used around ambient temperature. Please control the temperature to avoid frost or dew on the surface of EPD-panel. Moisture may ingress the EPD-panel and may damage the EPD-panel.

High temperature, high humidity, sunlight, or UV-light may degrade the EPD-panel's performance. Please do not expose the unprotected EPD-panel to high temperature, high humidity, sunlight, or UV-light for long periods of time. Please store the EPD panel in controllable environment of warehouse and in original package, without sunlight, without condensation.

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode the electronic components.

Do not disassemble or re-assemble the EPD-panel.

The EPD panel/module is manufactured from fragile materials such as glass and plastic and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating.

Minimise pulling or bending of the FPC and do not use the FPC for pick up. Do not press or pull FPC to ± 90° bending and don't twist FPC and PCB. Keep r ≥ 1mm when bending for assembly.

To avoid scratches, do not stack the EPD-panels/modules.

Do not apply pressure or hit to the EPD-module, IC, FPC and PCB to prevent damage.

Do not touch the FPC lead contacts and IC area to avoid ESD damage.

The display module is an electrostatic discharge (ESD) sensitive device. Ensure that proper ESD-precautions are in place to avoid damage of the display module.

Typical operation conditions in the assembly area are (25 ± 2)°C and 50%RH to 60%RH. Operators should use ionizer fan during assembly. The working area must be connected to ground, the resistance between operator and working area should be less than 5 Ω. Operator should wear PVC or anti-electrostatic gloves. Operators should wear grounding wrist ring and must make sure that grounding is fine. Before working in operation area, please ensure wrist ring and suit is fine by passing a conductive test before operation.

To avoid electrical overstress (EOS) in operation, please

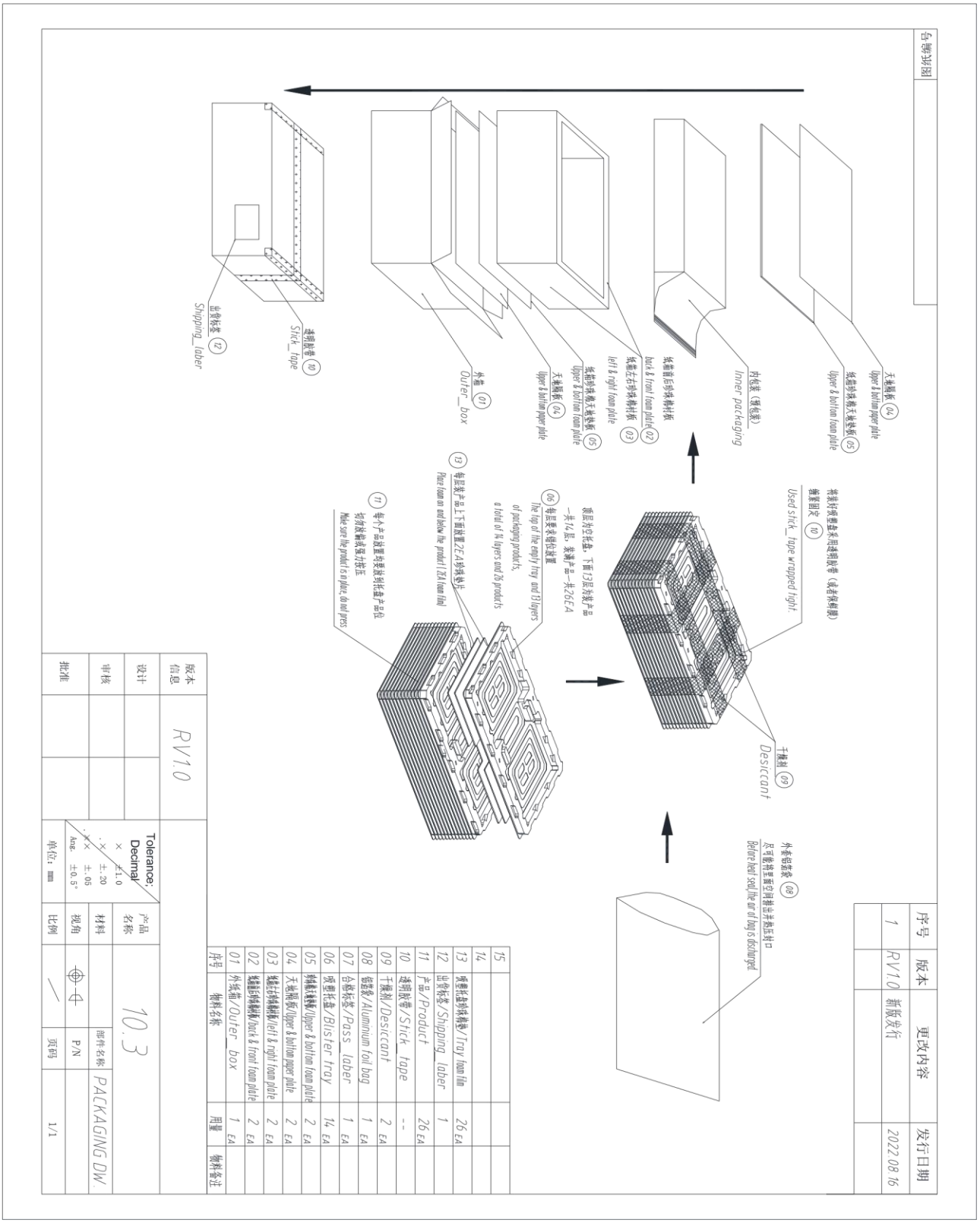
- ensure that power is off before EPD is installed into jig/tag
- ensure that FPC is well connected (no misalign in connector) to avoid a short
- do not remove/uninstall EPD from jig/tag when image is updating,
- switch power off after operation or function test before uninstalling the EPD

EOS or short may damage the IC or the TFT.

11. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

12. Packaging



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13. Mark and Bar Code Definition

OPM103E5 YYYYMMDD XX

YZC030AN1001001

A. OPM103E5: Module No.
B. YYYYMMDD: Product date year month day
C. XX: Internal Code
D. Bar Code definition

YZC030 A N 1 001 001

（1） （2） （3） （4） （5） (6)

1. O-Paper Film lot
2. Factory
3. Internal Code
4. Internal Code
5. Product lot
6. Product serial number

14. Inspection Standard

14.1 Appearances Inspection Standard

This appearance inspection shall be applied to EPD modules.

14.1.1 Inspection Conditions

Viewing Angle:	α = ± 45°
Viewing Distance:	30 cm ± 10 cm
Ambient Luminance:	700 ~ 1000 Lux
Supply Voltage:	typical value described on the electrical characteristics
Environment:	ambient temperature 20℃ ~ 25℃
ambient humidity	40 ~ 70%RH

ESD should be controlled within ± 200 V

14.1.2 Inspection Level: Level II

Sampling table: GB/T 2828.1-2012 II, unless otherwise agreed in writing.

14.1.3 Acceptance Quality Level (AQL)

major defect: 0.65

minor defect: 1.5

14.1.4 Classification of Defects

Defects are classified as either a major or a minor defect defined as below.

A major defect is a defect that is likely to result in failure or to significantly reduce the usability of the product for the intended function.

A minor defect is a defect that will not result in functional problems or classified deviations.

14.2 Quality Criteria

14.2.1 Zone Definitions

A-zone: EPD active area (not including border)
B-zone: out of active area

14.2.2 Appearances Criteria

The criteria are shown in the tables below. If any other items, values or applicable zones need to be required to be defined, a written agreement shall be signed, and otherwise a limited sample shall be made for reference.

Item	Description	Classification
No Image	No image shown on screen due to malfunction	Major
Line Missing	Line missing	Major
Abnormal Display	Unusual pattern or function displayed	Major
TFT Broken	TFT broken by external force	Major

Table 9: Major defects

Item		Criteria	Specific Zone	
Name	Description		A Zone	B Zone
Dot defect	spot, air bubble, foreign material in dot shape	D ⩽ 0.30 mm	Ignore	Ignore
		0.30 mm < D ⩽ 0.50 mm	⩽5	
		D > 0.50 mm	0	
Line defect	scratch on top surface, foreign material in line or spiral shape	L ⩽ 1.0 mm & W ⩽ 0.15mm	Ignore	Ignore
		1.0 mm < L ⩽ 5.0 mm & 0.15mm < W ⩽ 0.5 mm	⩽4	
		L > 5.0 mm or W > 0.5mm	0	
Chipping	corner chip	Do not affect the display, do not have diffuse or comminute cracks		
	edge chip			
Curl	curl for panel	⩽ 1.0 mm		

Table 10: Minor defects

A dot is defined as L ≤ 0.5 mm and L <4 W. Otherwise, it is a line defect, see Figure 10. A chip is a small area with missing material at the edges of the display module, see Figure 11.

Figure 10: line defect (left) and dot (right)

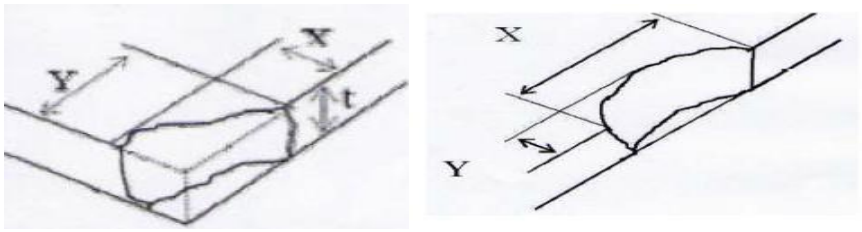

Figure 11: Corner chip (left) and edge chip (right)