E-PI
e-Paper Innovation

Specification

EPD-Module
Part-No. 70019803

10.7", 75 ppi, double sided driven, Colour

Revision 1.00

E-PI Confidential

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1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the electrophoretic display module, part number 70019803. It defines general characteristics of the display module and the technical information required to integrate the display module into a potential product.

The 70019803 is an active-matrix electrophoretic display (AM EPD), with interface and a reference system design. The module is a TFT-array driving EPD with integrated circuits including source and gate drivers. The 10.7" active area contains 1280 x 960 pixels that can be driven with 16 grey levels. Above this b/w-EPD, a colour filter array is positioned. Each colour pixel consists of a red, green, blue and white sub-pixel (RGBW) resulting in a colour resolution of 640 x 480 pixels. The module also includes a front light and a cover lens. The module can be used typically for an E-book reader.

1.2 Key features of display module

- Consists of an active-matrix electrophoretic display with source and gate drivers
- 640 x 480 colour pixels @ 340 µm pixel pitch
- Supports 4096 colours
- Incorporates industry-leading bi-stable electrophoretic display technology in pure reflective mode and with ultra-wide viewing angle
- Low power consumption
- Enables robust product design (glass-free)
- Display surface anti-glare and with hardcoat
- Usable in landscape and portrait mode

2. Mechanical specification

2.1 Dimensions

Parameter	Value	Unit	Comments
Active area size	10.7	inch	
Active area dimension	217.60 x 163.20	mm	
TFT-matrix	1280 x 960 150 170	Pixel ppi µm	b/w sub-pixels
Active area resolution	640 x 480 75 340	Pixel ppi µm	colour pixel.
Outline length	242.60 ± 0.2	mm	
Outline width	185.20 ± 0.2	mm	
Thickness	0.63 ± 0.1	mm	
Gate-FPC length	33.95 ± 0.3	mm	
Source-FPC length	43.15 ± 0.3	mm	
Weight	38	g	typical

Table 1: Mechanical specification

2.2 Outline

The outline of the final product is depicted in Figure 1.

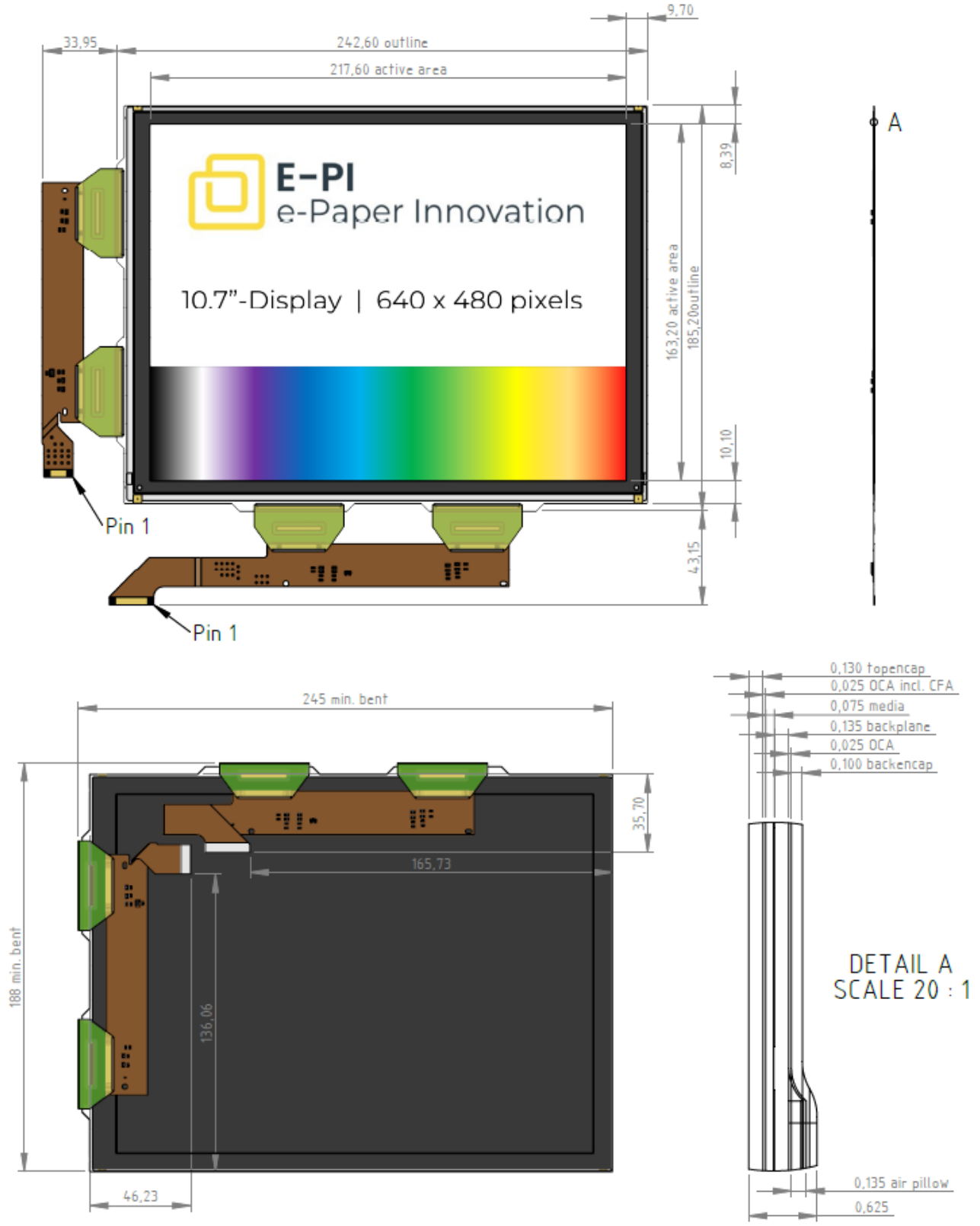

Figure 1: Dimensions of the final product in mm

2.3 Colour Filter Array

The colour display uses a RGBW colour filter array positioned directly above the front plane media surface, aligned with high accuracy to the backplane pixel structure.

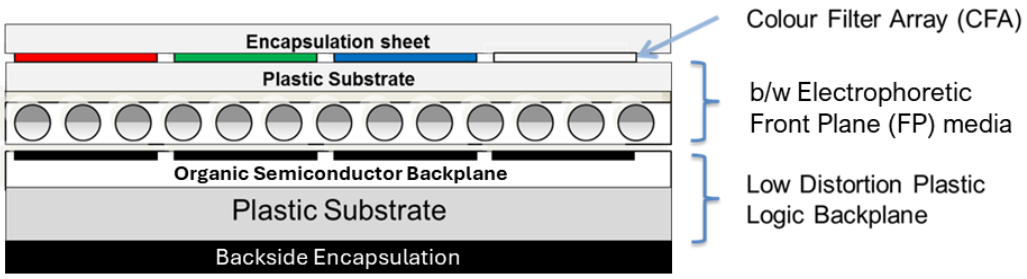

Figure 2: Schematic layer stack

The image below gives the arrangement of the sub-pixels in the colour filter which needs to be implemented in the controller settings/software. Primary colours are defined as colours created by driving the sub pixels to black and white only, not using any grey levels.

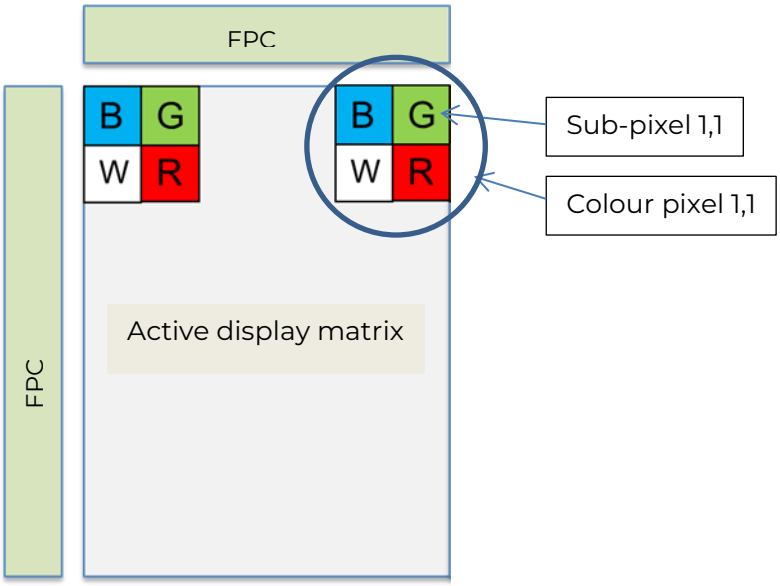

Figure 3: Arrangement of sub-pixels on the array

3. Optical specification

The display supports 4096 colour grades.

Grey levels are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and Lw are measured in % reflectance and Lw is defined as 100 %. This formula is valid for L* > 16. Measurements with front light switched on in emissive mode are listed in the CIE 1931 colour space.

3.1 Optical requirements

3.1.1 Picture quality

The display will be lineout free; however typical expectations are a pixel yield of > 99.99 %.

3.1.2 Parameters for GL waveforms

Measurements are done with a X-Rite i1 photo spectrometer or similar in the reflective respectively emissive mode for front light off/on. Measurement positions are 9 sites per display, see Figure 4.

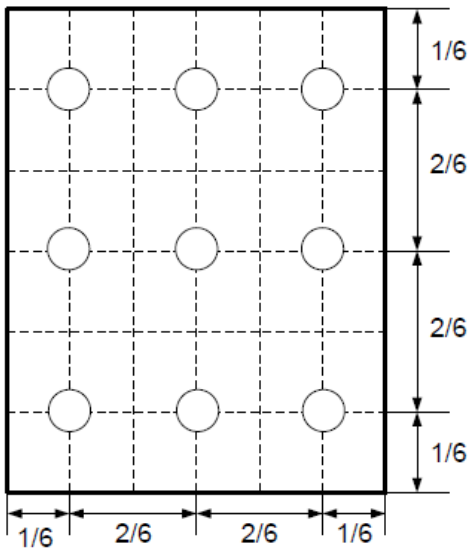

Figure 4: Measurement positions for optical parameters

Measurements are done with following parameters:

- viewing angle α = ± 45°
- viewing distance 30 cm ± 10 cm
- ambient luminance 700 ~ 1000 Lux for front light off; dark environment for front light on
- ambient temperature 20°C ~ 25°C
- ambient humidity 40%rH ~ 70%rH

Table 2 lists the criteria for the optical characterisation of the display module. The inspection is to be done after an image update with a GC16-waveform using the display specific settings as provided by E-PI (waveform, VCOM, ...). The measurement was done partly with a front light.

Front Light	Parameter	Description	Min	Typical	Max	Unit
Off	White state	Median GL15	50	53	-	L*
Off	Black state	Median GL0	-	14	18	L*
Off	Contrast ratio	Black to White	10:1	13:1		
Off	colour	NTSC	1.2	2.5		%
On	Brightness	@ 20 mA [1]	80	100	-	cd/m^2
On	White chromacity x		0.27	0.31	0.35	-
On	White chromacity y		0.29	0.33	0.37	-
On	Luminance uniformity	9-point measurement [2]	60	75	-	%
On	Contrast ratio	Black to White [3]	7:1	10:1	-	-

Table 2: Optical parameters

Notes:

1. Brightness is measured after front light is turned on with I = 20 mA and stabilised, measured with X-rite I1 in emissive mode
2. Uniformity is defined as:
   (Minimum brightness of 9 testing points) / (Maximum brightness of 9 testing points)
3. Definition of contrast ratio with front light on:
   (Luminance when display is driven to white) / (Luminance when display is driven to black)

3.1.3 Display update waveforms

The display module will be supplied with a library of waveforms that are tuned to optimise the display performance. Each waveform has an optimum temperature range over which it is valid – it is the responsibility of the display controller and software to ensure that the correct waveform out of the library is selected for the current display module temperature.

Waveforms can be stored in the SPI-Flash on the gate FPC. As default, the SPI-Flash is empty but waveforms can be pre-programmed on customer request. The waveform format is specific to used EPDC.

E-PI will provide the waveforms that support full screen updates as well as fast updates, see Table 3.

Mode Name	Usage	Grey Levels	Ghosting	Update speed
INIT	Recover from unknown state/ start up	White only	Low	Slow
GC16	Full refresh	All colours	Low	Slow
DU	Delta Update; 16GL to Monochrome	All colours → primary colours	High	Medium
A2	Fast monochrome updates	primary colours → primary colours	High	Fast

Notes: additional customer specific waveforms are possible on request

Table 3: Waveform types

4. Reliability and other specifications

Parameter	Value	Unit	Comments
Operating Temperature	0 to 50	°C	The operating temperature of 0 to 50 °C is a limitation of the media material
Storage Temperature	-25 to 50	°C	
Operation/Storage humidity	25 to 60	%rH	T ≤ 40°C without dewing
Waterproofing	n/a		The deliverables of this product will not guarantee an IP-rating
FPC tail minimum internal bend radius	0.7	mm	with E-Z fold design
COF minimum internal bend radius	0.4	mm	bending not permitted at IC location.

Table 4: Reliability parameters

No.	Test	Condition	Comments
1	High Temperature Operation	T = +60°C, RH = 30 % for 240 hrs	IEC 60 068-2-2Bp
2	Low Temperature Operation	T = 0°C for 240 hrs (RWU-profile)	IEC 60 068-2-2Ab
3	High Temperature Storage	T = +70°C, RH = 23 % for 240 hrs	IEC 60 068-2-2Bp
4	Low Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab
5	High Temperature, High Humidity Operation	T = +40°C, RH = 90 % for 360 hrs (RWU-profile)	IEC 60 068-2-3CA
6	High Temperature, High Humidity Storage	T = +60°C, RH = 90 % for 360hrs	IEC 60 068-2-3CA
7	Thermal Shock	Cycle: [-25°C/30min] → [+70°C/30 min] 100 cycles	IEC 60 068-2-14
8	Real World Use	T = +22°C for 500hrs T = +40°C for 500hrs	RWU-profile
9	Ambient Operation	T = +22°C for 1 Mio updates	1s image updates
10	Electrostatic Effect (nonoperating)	Machine model +/- 250 V, 0 Ω, 200 pF	IEC 62179, IEC 62180

Table 5: Reliability tests; at the end of the test, electrical, mechanical, and optical specifications shall be fulfilled

5. Electrical Specification

5.1 Connection of display module

The Display requires two electrical connectors to connect it to the driver electronics.

- FPC thickness: 0.3 mm ± 0.05 mm
- Connection pitch: 0.5 mm
- Contact location: Bottom contact (once tail is folded)
- Number of connect pins: 26 for Gate
  40 for Source

Recommended connectors are HRS FH12-26S-0.5SH and FH12-40S-0.5SH or compatible ones. A top contact connector is required if the connection tails are not folded. Please note that folding the tails reverses the connection order.

5.2 Electrical pin-out of display module

Pin	Symbol	Description
1	GND	Ground
2	VCOM	Common voltage
3	VBORDER	Voltage border electrode (currently not supported by display)
4	GD_AD	Active Discharge
5	GD_DIR	Scan Direction
6	VDD	Logic power supply
7	VDD	Logic power supply
8	GD_OE	Mode / Output Enable
9	GND	Ground
10	GD_CLK	Gate Clock
11	GD_SPV2	Shift register start pulse
12	GND	Ground
13	VGH	HV power supply for gate positive
14	VGH	HV power supply for gate positive
15	GND	Ground
16	VGL	HV power supply for gate negative
17	VGL	HV power supply for gate negative
18	GND	Ground
19	SPI_MOSI	SPI Master Out Slave In
20	SPI_CLK	SPI Clock
21	SPI_MISO	SPI Master In Slave Out
22	SPI_CE	SPI Chip Enable
23	GD_SPV1	Shift register start pulse
24	VBORDER	Voltage border electrode (currently not supported by display)
25	VCOM	Common voltage

Pin	Symbol	Description
26	GND	Ground

Table 6: Electrical pin-out for the gate-FPC

Pin	Symbol	Description
1	VCOM	Common voltage
2	GND	Ground
3	VDD	Logic power supply
4	VDD	Logic power supply
5	GND	Ground
6	VNEG	Negative power supply for driver
7	VNEG	Negative power supply for driver
8	GND	Ground
9	VPOS	Positive power supply for driver
10	VPOS	Positive power supply for driver
11	GND	Ground
12	SD_STL2	Shift register start pulses / Chip Enable
13	SD_ISEL	Input data bus width selection (8 / 16 bit)
14	SD_SHR	Shift Direction
15	SD_OE	Source Output Enable
16	SD_LE	Latch Enable
17	SD_D15	Input Data Line
18	SD_D14	Input Data Line
19	SD_D13	Input Data Line
20	SD_D12	Input Data Line
21	SD_D11	Input Data Line
22	SD_D10	Input Data Line
23	SD_D9	Input Data Line
24	SD_D8	Input Data Line
25	GND	Ground
26	SD_CLK	Source Clock
27	GND	Ground
28	SD_D7	Input Data Line
29	SD_D6	Input Data Line
30	SD_D5	Input Data Line
31	SD_D4	Input Data Line
32	SD_D3	Input Data Line
33	SD_D2	Input Data Line
34	SD_D1	Input Data Line

Pin	Symbol	Description
35	SD_D0	Input Data Line
36	SD_STL1	Shift register start pulses / Chip Enable
37	GND	Ground
38	VBORDER	Voltage border electrode (connect to VCOM via 10k resistor)
39	VCOM	Common voltage
40	GND	Ground

Table 7: Electrical pin-out for the source-FPC

6. Electrical Characteristics

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings. Exceeding these ratings as well as longer term operation outside the recommended ratings may result in permanent damage of the display module.

Parameter	Symbol	Rating	Unit
Logic power supply	VDD	-0.3 ~ +4.0	V
HV power supply for gate positive	VGH	-0.3 ~ +40	V
HV power supply for gate negative	VGL	-50 ~ +0.3	V
Maximum gate voltage range	VGH-VGL	80	V
HV power supply for source positive	VPOS	-0.3 ~ +18	V
HV power supply for source negative	VNEG	-18 ~ +0.3	V
Maximum source voltage range	VPOS-VNEG	36	V

Table 8: Absolute maximum ratings

6.2 Panel DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal ground	GND	-	0	-	V
Logic power supply	VDD	3.0	3.3	3.6	V
HV power supply for gate positive	VGH	26	28	30	V
HV power supply for gate negative	VGL	-44	-42	-40	V
HV power supply for source positive	VPOS	14.6	15	15.4	V
HV power supply for source negative	VNEG	-15.4	-15	-14.6	V
Asymmetry source (VPOS+VNEG)	VASYM	-150	0	150	mV
Common voltage	VCOM *	1	5.0	9	V

* VCOM is needed to be tuned for each display module. The correct value will be supplied as part of the waveform data.

Table 9: Panel DC characteristics

6.3 Power On/Off-Sequence

6.3.1 Power Supply Start Up Sequence

- Initial state: all supplies off (disabled).
- Enable VDD, the source and gate driver logic supplies and allow to stabilize.
- Set SD_OE=0 to set all source outputs to 0V (GND).
- Set GD_OE=0 to set all gate outputs to VGH.
- Open VCOM switch to isolate the display VCOM electrode from the VCOM supply.
- Enable HV supplies in sequence VGH, VCOM, VGL, VNEG, VPOS (see drawing below)
- Allow supplies to stabilize.
- Enable source and gate driver outputs by SD_OE=GD_OE=1.
- Write one null frame to the display.
- Close the VCOM switch.

6.3.2 Display Image Update

- Write image update data to the display system.
- A final null frame is required as part of the image update (this will be supplied as part of the waveform data).

6.3.3 Power Down Sequence

- Open the VCOM switch.
- Disable source and gate outputs by SD_OE=GD_OE=0.
- Shut down the HV power supplies in the reverse order of Power up sequence and allow to go to 0V (GND) (Active discharge recommended).
- Disable VDD.

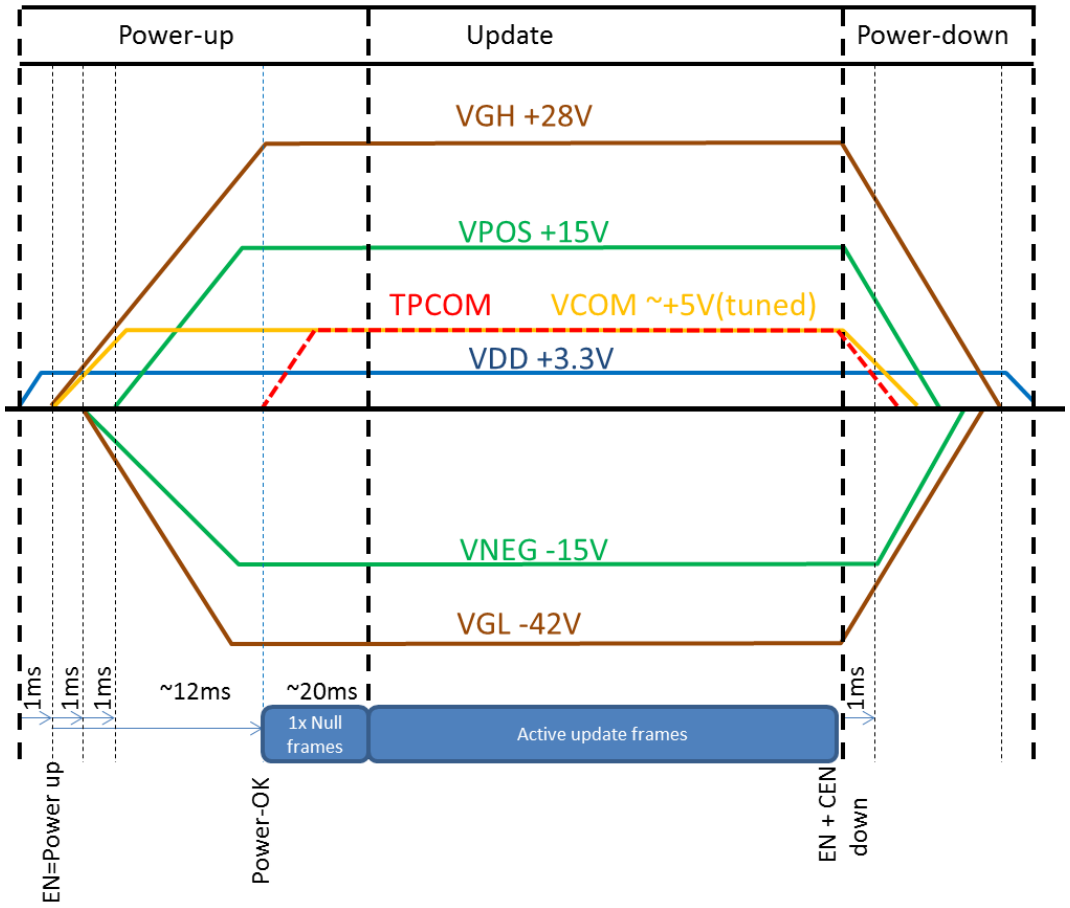

Figure 5: Power up/down sequence

6.4 AC-Characteristics

For details of AC-timing please also check the data sheets of the driver chips UC8124 (source) and UC8434 (gate).

7. Handling requirements

The display modules are shipped in appropriate packages. All loose tails must be constrained during shipping.

Keep the EPD-panel/module in the specified environment and original packing boxes when stored to avoid scratching and to keep original performance.

The product is intended to be used around ambient temperature. Please control the temperature to avoid frost or dew on the surface of EPD-panel. Moisture may ingress the EPD-panel and may damage the EPD-panel.

High temperature, high humidity, sunlight, or UV-light may degrade the EPD-panel's performance. Please do not expose the unprotected EPD-panel to high temperature, high humidity, sunlight, or UV-light for long periods of time. Please store the EPD panel in controllable environment of warehouse and in original package, without sunlight, without condensation.

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode the electronic components.

Do not disassemble or re-assemble the EPD-panel.

The EPD panel/module is manufactured from fragile materials such as glass and plastic and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating.

Minimise pulling or bending of the FPC and do not use the FPC for pick up. Do not press or pull FPC to ± 90° bending and don't twist FPC and PCB. Keep r ≥ 1mm when bending for assembly.

To avoid scratches, do not stack the EPD-panels/modules.

Do not apply pressure or hit to the EPD-module, IC, FPC and PCB to prevent damage.

Do not touch the FPC lead contacts and IC area to avoid ESD damage.

The display module is an electrostatic discharge (ESD) sensitive device. Ensure that proper ESD-precautions are in place to avoid damage of the display module.

Typical operation conditions in the assembly area are (25 ± 2)°C and 50%RH to 60%RH. Operators should use ionizer fan during assembly. The working area must be connected to ground, the resistance between operator and working area should be less than 5 Ω. Operator should wear PVC or anti-electrostatic gloves. Operators should wear grounding wrist ring and must make sure that grounding is fine. Before working in operation area, please ensure wrist ring and suit is fine by passing a conductive test before operation.

To avoid electrical overstress (EOS) in operation, please

- ensure that power is off before EPD is installed into jig/tag
- ensure that FPC is well connected (no misalign in connector) to avoid a short
- do not remove/uninstall EPD from jig/tag when image is updating,
- switch power off after operation or function test before uninstalling the EPD

EOS or short may damage the IC or the TFT.

8. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.