Specification

EPD-Module
Part-No. 70004001

2.1", 132 ppi, single sided driven, Colour

Revision 1.00

E-PI Confidential

Title	EPD-Module – Part-No. 70004001
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Document Type	Specification
Document Reference	
Date	May 29, 2024
Revision	1.00

Revision	Date	Description
1.00	29-May-2024	Initial release

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1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the electrophoretic display module with colour media, part number 70004001. It defines general characteristics of the display module and the technical information required to integrate the display module into a potential product.

The 70004001 is an active-matrix electrophoretic display (AM EPD), with interface and a reference system design. The 2.1" active area contains 240 x 146 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate driver, source driver and an integrated EPD-controller. The module can be used in portable electronic devices e.g. in credit cards.

1.2 Key features of display module

- Consists of an active-matrix electrophoretic display driven by one chip combining source drivers, gate drivers and an integrated EPD-controller bonded directly on the display substrate (COP = chip on plastic)
- 240 x 146 pixels @ 192 µm pixel pitch
- Supports black and white as well as the colours red, blue, green and yellow
- The full refresh time is 15 seconds
- Display surface anti-glare and hardcoat (2H)
- Incorporates industry-leading bi-stable electrophoretic display technology in pure reflective mode and with ultra-wide viewing angle
- Enables robust product design (glass-free and flexible)
- SPI-interface to customer application

2. Mechanical specification

2.1 Dimensions

Parameter	Value	Unit	Comments
Active area size	2.1	inch	
Active area dimension	46.08 x 28.03	mm	
Active area resolution	240 x 146 132	Pixel ppi	
Active area pixel pitch	192	µm	
Outline length	53.28 ± 0.2	mm	
Outline width	38.33 ± 0.2	mm	
Thickness	0.53 ± 0.1	mm	
FPC length	16.00 ± 0.3	mm	length over display outline
Weight	1.7	g	typical

Table 1: Mechanical specification

2.2 Outline

The outline of the final product is depicted in Figure 1.

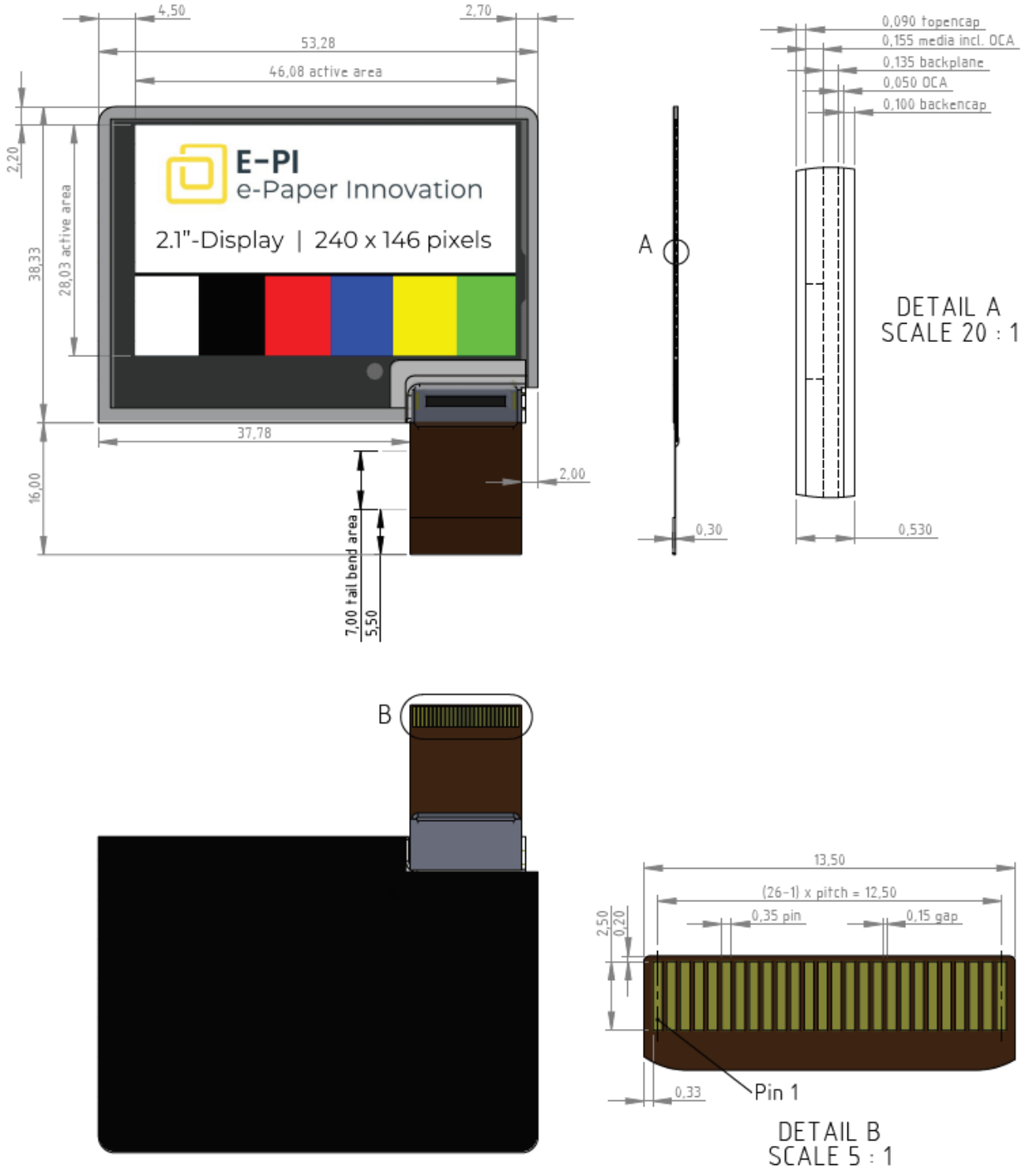

Figure 1: Dimensions of the final product in mm

3. Optical specification

The display supports natively black and white.[1] Specific display grey levels are defined using the terminology GLx, where x = 0-15. GL0 corresponds to “black” and GL15 corresponds to “white”.

Grey levels are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and Lw are measured in % reflectance and Lw is defined as 100 %. This formula is valid for L* > 16.

Measurements are made with illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

3.1 Optical requirements

3.1.1 Picture quality

The display will be lineout free; however typical expectations are a pixel yield of > 99.99 %.

3.1.2 Parameters for GL waveforms

Parameter	Description	Min	Typical	Max	Unit
White state	Median GL15	62	70	-	L*
Black state	Median GL0	-	24	30	L*
Red colour					
Blue colour					
Green colour					
Yellow colour					

Note: The reflectance and contrast ratio is measured between 0°C and 40°C at 50%rH. Reflectance measurements are done using a spectrophotometer. E-PI is using the “spectro guide” from BYK-Gardner GmbH.

Table 2: Optical requirements

3.1.3 Display update waveforms

The display module will be supplied with a library of waveforms that are tuned to optimise display performance at ambient temperature. The waveform library will be stored into an on-board flash memory.

E-PI will provide the waveforms that support full screen updates.

[1] Waveforms to drive 4 grey levels are available

4. Reliability and other specifications

Parameter	Value	Unit	Comments
Operating Temperature	0 to 50	°C	The operating temperature of 0 to 50 °C is a limitation of the media material
Storage Temperature	-25 to 50	°C	
Operation/Storage humidity	25 to 60	%RH	T ≤ 40°C without dewing
Waterproofing	n/a		The deliverables of this product will not guarantee an IP rating

Note: long-term exposure of stress close to the limits might reduce the overall lifetime

Table 3: Reliability parameters

No.	Test	Condition	Comments
1	High Temperature Operation	T = +60°C, RH = 30 % for 240 hrs	IEC 60 068-2-2Bp
2	Low Temperature Operation	T = 0°C for 240 hrs (RWU-profile)	IEC 60 068-2-2Ab
3	High Temperature Storage	T = +70°C, RH = 23 % for 240 hrs	IEC 60 068-2-2Bp
4	Low Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab
5	High Temperature, High Humidity Operation	T = +40°C, RH = 90 % for 360 hrs (RWU-profile)	IEC 60 068-2-3CA
6	High Temperature, High Humidity Storage	T = +60°C, RH = 90 % for 360hrs	IEC 60 068-2-3CA
7	Thermal Shock	Cycle: [-25°C/30min] → [+70°C/30 min] 100 cycles	IEC 60 068-2-14
8	Real World Use	T = +22°C for 500hrs T = +40°C for 500hrs	RWU-profile
9	Ambient Operation	T = +22°C for 1 Mio updates	1s image updates
10	Electrostatic Effect (nonoperating)	Machine model +/- 250 V, 0 Ω, 200 pF	IEC 62179, IEC 62180

Table 4: Reliability tests; at the end of the test, electrical, mechanical, and optical specifications shall be fulfilled

5. Electrical specification

5.1 Connection of display module

The display module can be contacted by a FPC bonded to the backplane. The contacts are on the backside of the FPC. Dimensions are shown in Figure 1. On the connector side, The FPC has a 4.5 mm deep stiffener resulting in a 0.3 mm thick FPC on the connector side. There are 26 Pins having a pitch of 0.5 mm.

5.2 Electrical pin-out of display module

No.	Name	I/O	Description
1,2	VSL	O	Negative source voltage, connect to capacitor
3,4	VSH	O	Positive source voltage, connect to capacitor
5,6	VGL	I	Negative gate voltage, input from booster
7,8	VGH	I	Positive gate voltage, input from booster
9	GDR_P	O	P-MOS booster gate control
10	GDR_N	O	N-MOS booster gate control
11	VDDIO	P	Interface power connect to VDDA for 3.3V I/O, connect to VDD for 1.8V I/O
12	VDDA	P	Analog power
13	SPI_MISO	O	SPI data output
14	SPI_MOSI	I	SPI data input
15	SPI_CLK	I	SPI clock
16	SPI_CS	I	SPI chip select
17	RST_N	I	Global reset, low active When RST_N becomes low, driver will reset. All registers will be reset to default value and all driver functions will be disabled. SD output and VCOM will base on previous condition; they may have two conditions: 0V or floating.
18	BUSY_N	O	BUSY pin - indicates the driver status. L: Controller / Driver is busy H: non-busy. Host side can send command/data to driver.
19	GND	P	Ground
20,21	VDD	P	Core Logic Power VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and GND.
22	VDDA	P	Analog power
23	EXTVDD	I	Controls internal regulator for VDD EXTVDD connected GND: internal regulator is on. EXTVDD connected VDDA: internal regulator is off, need an external 1.8V supply to VDD.
24,25	GND	P	Ground
26	TPCOM	O	Connect to capacitor

I = Input Pin O =Output Pin P = Power Pin

Table 5: Electrical pin-out to connect the display module

Reference connector is the Omron XF2M-2615-1A, 26-pin Rotary Backlock Connector or Hirose FH34SRJ-26S-0.5SH(50), both dual contact, 0.5 mm pitch.

5.3 Controller

The display is driven and controlled by the UC8156 which is an all-in-one EPD driver and timing controller from Ultrachip. This chip is bonded to the Plastic Logic display substrate via a bonding technology called “Chip on Plastic” (COP).

Please refer to Ultrachip UC8156 datasheet for the full controller specification.

5.4 Display power consumption

The power consumption is very much depending on the finally implemented waveform. Typical values are given in Table 6.

Mode	Parameter	Typical	Maximum	Unit
Operation	Mean current for “typical” image update	6.0		mA
Operation	Mean current for a “worst case” image update	15		mA
Operation	Peak current	160	300	mA
Stand-by with HV’s on	Stand-by current 1	4		mA
Stand-by with HV’s off	Stand-by current 2	30		µA
Sleep	Sleep current	0.7	0.8	µA

Note (1): see detailed conditions, measurement setup and value calculation below
Note (2): peak current duration ~ 10 µs

Table 6: Power consumption of the display module

5.4.1 Measurement conditions

The measurement is done at ambient conditions, around 23°C and 50%RH. Latest register settings and operation sequences are used and waveform and VCOM-value is already programmed into the controller’s internal memory.

The “worst case” image update with regards to the power consumption is the change from stripe pattern to inverse stripe pattern:

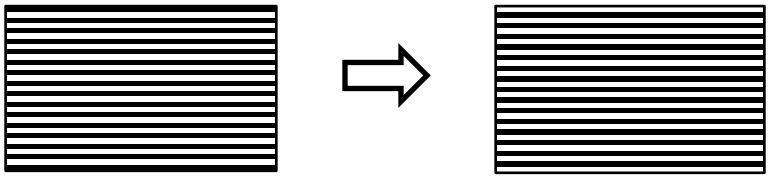

Figure 2: Image update for power consumption worst case

5.4.2 Measurement setup

The power consumption specifications were determined by utilizing high side current measurements on the supply power line of the displays. The current rating is detected by measuring the voltage drop over a 0.01 Ω shunt resistor applying a burden voltage of 10 µV/mA to the display and sub-sequentially amplifying the signal with an ultra-low offset/drift, low noise precision amplifier. The amplified signal Is either detected by an oscilloscope sampling the signal with 2.5 MS/s or a digital multimeter. The measurement setup is shown in Figure 3.

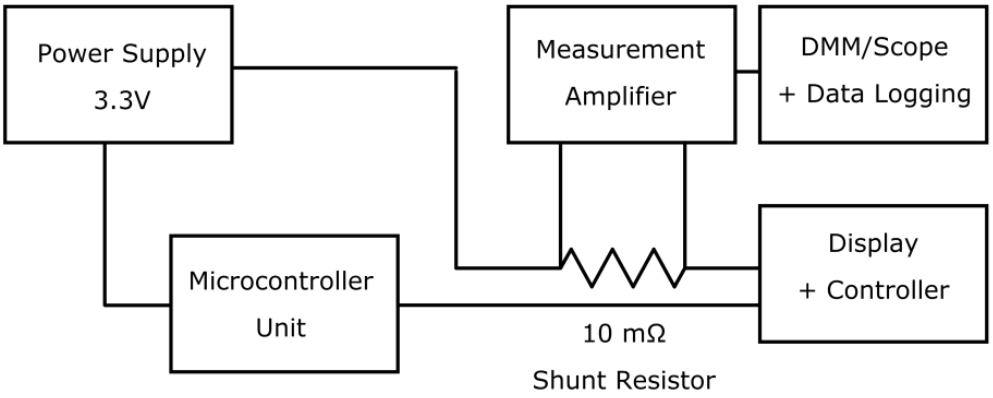

Figure 3: Measurement setup

5.4.3 Value calculation for mean power

The “input current” value is calculated as the average value over the whole update (approx. BUSY high time). The given value includes the consumption of the display and the complete external display related electronic (HV generation).

6. Application reference circuit for display module

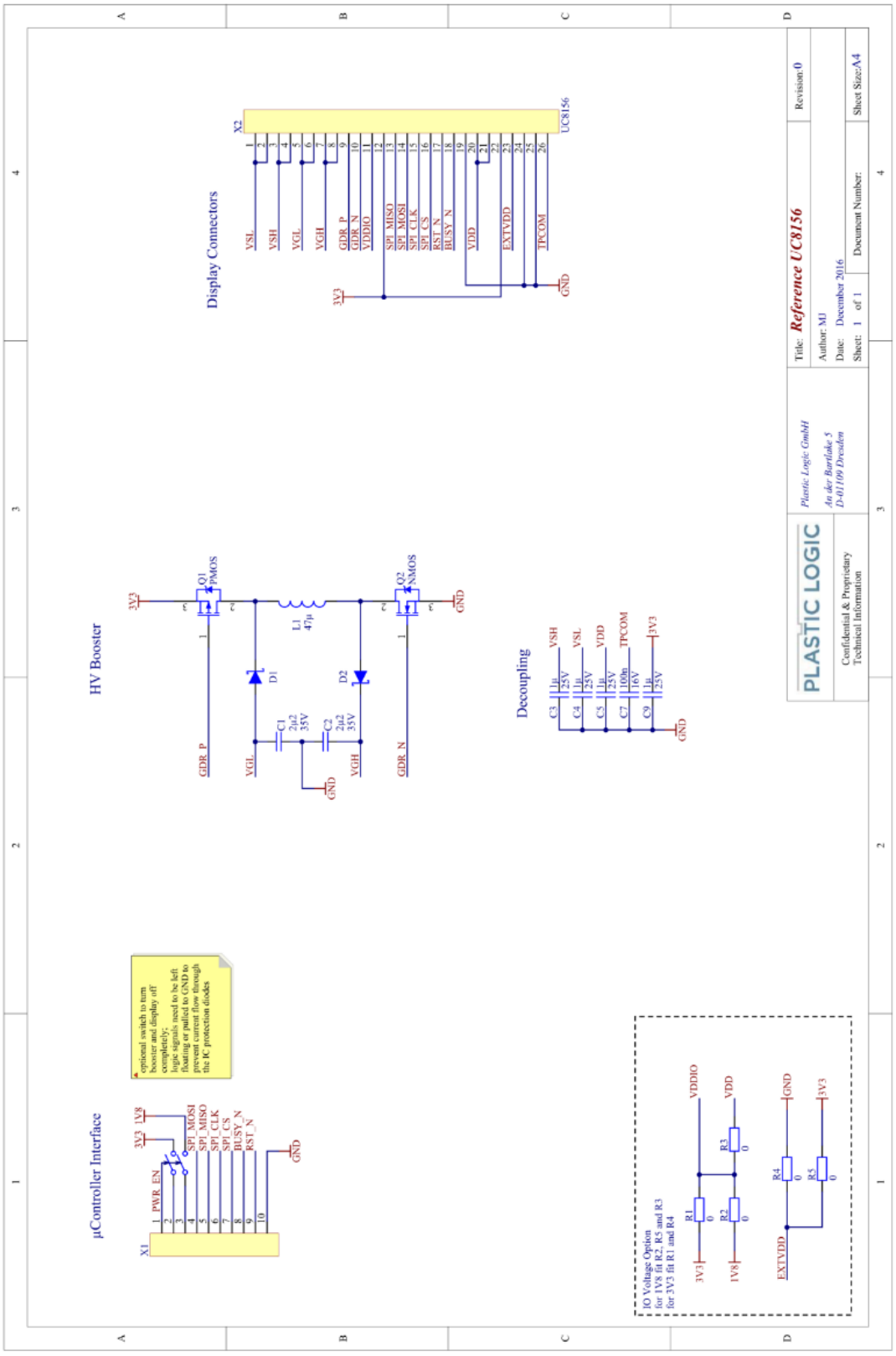

Figure 4: Reference circuit

Components	Value/Type	Requirements
C1-C2	2.2 μF	Dielectric：X5R/X7R, Rated Voltage：35 V
C3-C5, C9	1.0 μF	Dielectric：X5R/X7R, Rated Voltage：25 V
C7	100 nF	Dielectric：X5R/X7R, Rated Voltage：16 V
D1-D2	Diode	MBR0530 (1. reverse DC ≥ 30 V / 2. Io ≥ 500 mA / 3 .forward ≤ 430 mV)
R1-R5	Ω	1 %
Q1	PMOS	Si1304BDL 1.Drain Source breakdown voltage ≥ 30 V 2.Vgs(Vth) = 0.9 V（TYP）,1.3 V(Max) 3. Rds on ≤ 2.1 Ω @Vgs = 2.5 V
Q2	NMOS	Si1304BDL 1.Drain Source breakdown voltage ≥ 30 V 2.Vgs(Vth) = 0.9 V（TYP）,1.3 V(Max) 3. Rds on ≤ 2.1 Ω @Vgs = 2.5 V
L1	47 μH	CDRH2D18/LDNP-470NC, Io = 500(Max)

Table 7: Reference components

7. Handling requirements

The display modules are shipped in appropriate packages. All loose tails must be constrained during shipping.

Keep the EPD-panel/module in the specified environment and original packing boxes when stored to avoid scratching and to keep original performance.

The product is intended to be used around ambient temperature. Please control the temperature to avoid frost or dew on the surface of EPD-panel. Moisture may ingress the EPD-panel and may damage the EPD-panel.

High temperature, high humidity, sunlight, or UV-light may degrade the EPD-panel's performance. Please do not expose the unprotected EPD-panel to high temperature, high humidity, sunlight, or UV-light for long periods of time. Please store the EPD panel in controllable environment of warehouse and in original package, without sunlight, without condensation.

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode the electronic components.

Do not disassemble or re-assemble the EPD-panel.

The EPD panel/module is manufactured from fragile materials such as glass and plastic and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating.

Minimise pulling or bending of the FPC and do not use the FPC for pick up. Do not press or pull FPC to ± 90° bending and don't twist FPC and PCB. Keep r ≥ 1mm when bending for assembly.

To avoid scratches, do not stack the EPD-panels/modules.

Do not apply pressure or hit to the EPD-module, IC, FPC and PCB to prevent damage.

Do not touch the FPC lead contacts and IC area to avoid ESD damage.

The display module is an electrostatic discharge (ESD) sensitive device. Ensure that proper ESD-precautions are in place to avoid damage of the display module.

Typical operation conditions in the assembly area are (25 ± 2)°C and 50%RH to 60%RH. Operators should use ionizer fan during assembly. The working area must be connected to ground, the resistance between operator and working area should be less than 5 Ω. Operator should wear PVC or anti-electrostatic gloves. Operators should wear grounding wrist ring and must make sure that grounding is fine. Before working in operation area, please ensure wrist ring and suit is fine by passing a conductive test before operation.

To avoid electrical overstress (EOS) in operation, please

- ensure that power is off before EPD is installed into jig/tag
- ensure that FPC is well connected (no misalign in connector) to avoid a short
- do not remove/uninstall EPD from jig/tag when image is updating,
- switch power off after operation or function test before uninstalling the EPD

EOS or short may damage the IC or the TFT.

8. Safety and flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

9. Compatible evaluation kits

Do not use any other evaluation kit than the recommended one.